Part 4 of Extra Material for use with

PSpice®
Simulation of Power Electronics Circuits

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Contents

See Appendix E in the book.

10.4 INTEGRAL-CYCLE CONVERTERS

Integral-cycle converters can perform direct ac to ac conversion without intermediate ac-dc, dc-ac conversion and it can be accomplished with lossless switching. See PESS Fig. 1.5.

The basis of integral-cycle control is that a sinusoid can be approximated by combining and removing half cycles from a higher frequency ac source. Since only half or full cycles are ever used, the converter switches are turned on or off only during half-cycle boundaries at which the input voltage passes through zero. As a result, these converters achieve zero-voltage switching without the need for a resonant circuit. This is demonstrated in the following examples.

EXAMPLE W10.4.1

Figure W10.4.1a illustrates a simple integral-cycle controller. This figure comprises the source, the load, and the power switch which performs the conversion. In this particular example we desire to reduce the source frequency by a factor of three. Determine a suitable switching sequence and simulate using PSpice. Display the resulting load voltage using PROBE. Determine the total harmonic distortion THD of the output voltage.

Solution

This is a general example with many free choices for parameter values.
There are four steps to achieve a solution.

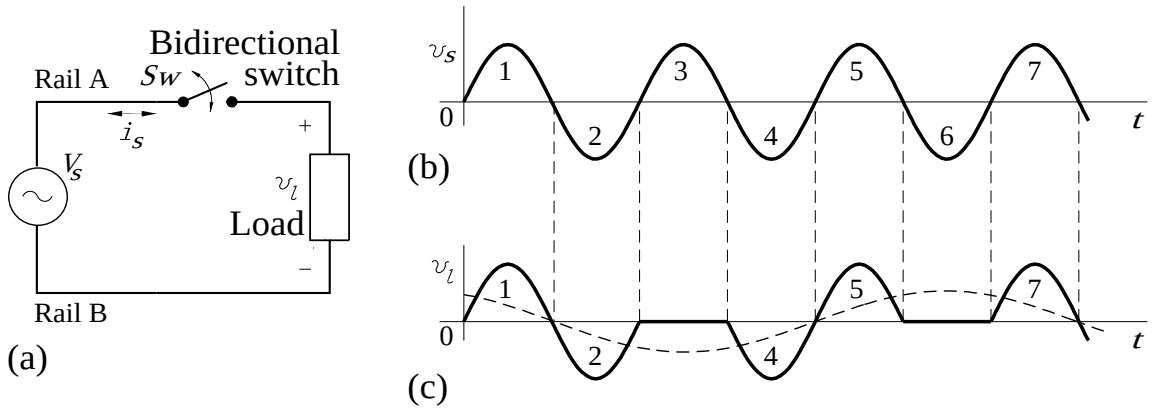

Fig. W10.4.1 Integral-cycle control.
(a) Circuit diagram, (b) source voltage, (c) load voltage.

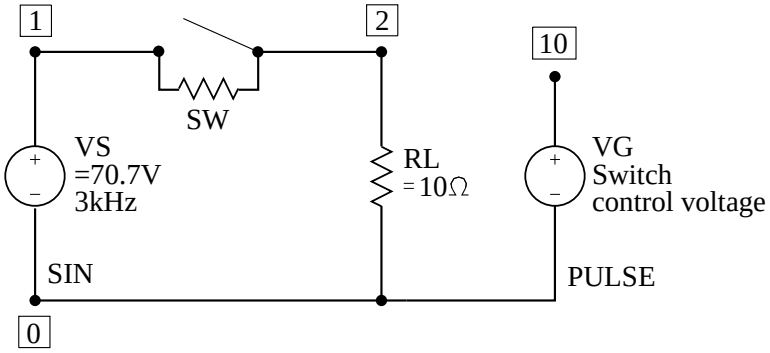

Fig W10.4.1d PSpice configuration, integral-cycle control.

STEP 1

A switching sequence for the bidirectional switch must be devised first. One possibility is a switching sequence that removes every third half-cycle. Figure W10.4.1b shows the waveform of the ac source voltage. If every third half-cycle is removed, the load voltage will resemble Fig. W10.4.1b minus the third and sixth half cycles. See Fig. W10.4.1c. Although the resulting load voltage is far from a perfect sinusoid, it is one-third the frequency of the ac source. Because of the blocked half-cycles, the effective load voltage will be reduced. In addition, in order that the load response to the blocked half-cycles is minimal instant-aneously, but acceptable on average, the frequency of the supply must be sufficiently high.

STEP 2

The next step is to transform the diagram in Fig. W10.4.1a into a PSpice configuration. See Fig. W10.4.1d. This circuit has only four nodes. Because the switch SW operates on a simple periodic squarewave, a PULSE source may be used for the switch's control voltage. The circuit file is shown below.

» » » » W10_4_1.CIR »

```
INTEGRAL-CYCLE AC-AC CONVERTER
* A converter with lossless switching.

* The POWER library is used for the switch model.
.LIB     POWER.LIB
.INC     OPTIONS;                                  Convergence aid.

* PARAMETERS
.PARAM  FREQ=3kHz   PERIOD={1/FREQ};               AC source frequency.
.PARAM  VRMS=70.7V  VMAX={SQRT(2)*VRMS};           Source voltage.
.PARAM  RLOAD=10ohms;                              Load resistance.
```

```
* SOURCES
VS     1  0  SIN(0  {VMAX}  {FREQ}  0  0  0)
VSIN   11   0   SIN(0  {3*VMAX}  {FREQ/3}  0  0  -240);   Sinewave at 1kHz.
VG     10   0   PULSE(0  1V  0  2ns  2ns  {PERIOD-4ns}  {3*PERIOD/2})

* CIRCUIT ELEMENTS
SW     1  2  10  0   SWITCH;                SWITCH parameters in POWER.LIB.
RL     2  0  {RLOAD};                       Output load resistance.

* ANALYSIS
.FOUR   1kHz  15 v(2);                      Fourier analysis of output waveform.
.TRAN   5us   2ms;                          Two load cycles.
.PROBE
.END
```

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STEP 3 The third step is to run the PSpice program with the circuit file W10_4_1.CIR.

STEP 4 The fourth step is to run PROBE with W10_4_1.DAT and view the results. See Fig. W10.4.1e. The load voltage is an alternating voltage source missing every third half-cycle of the supply waveform. The load voltage distortion of 170.3% is obtained from EX10_4_1 .OUT.

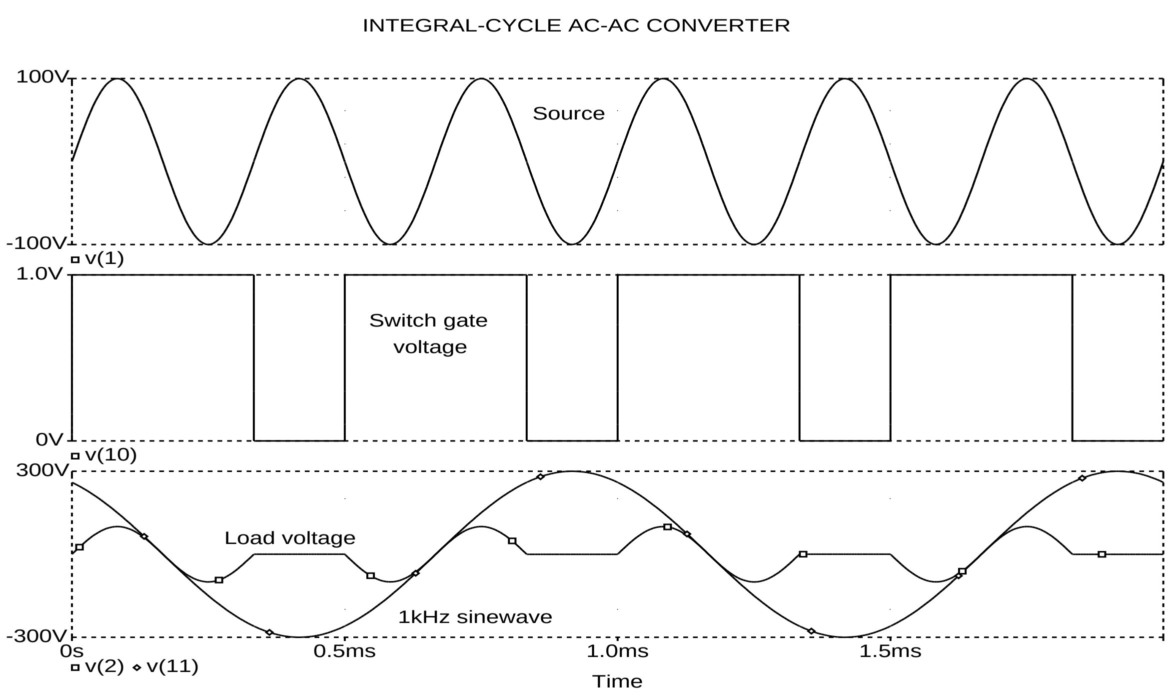

Fig. W10.4.1e

END OF EXAMPLE W10.4.1

Drill Exercise WD10.4.1
Consider EXAMPLE W10.4.1 and add a parallel inductance 100μH to the existing load resistance. Simulate using PSpice and plot the resulting load- resistance current and the inductor current.

Drill Exercise WD10.4.1a
Consider the ac-ac converter illustrated in Fig. W10.4.1a. The circuit has the following specifications.

$V_s = 50$V(rms) at 200kHz, bidirectional switch, $R_l = 5\Omega$.
Load-voltage frequency 40kHz (symmetrical waveform).

Follow the pattern of EXAMPLE W10.4.1 and do a PSpice simulation. Plot traces of the supply and the load voltages. Determine **(a)** the rms value of the load voltage, **(b)** the fundamental rms value of the load voltage and **(c)** the total harmonic distortion THD of the load-voltage waveform.
(Ans: **(a)** 31.6V, **(b)** 7.77V, **(c)** 393.0%.)

The previous example was a simple introduction to the concept of integral-cycle converters. Since all switching occurs during the zero-crossing of the source voltage there should be lossless switching. Also, this technique results in a load-voltage waveform with substantial distortion and a reduced voltage. Because only a single switch is used in EXAMPLE W10.4.1, there are significant limitations to its use.

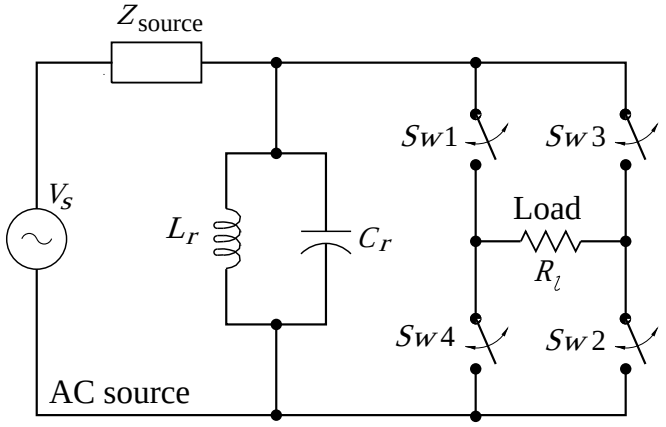

Fig. 10.4.1
Single-phase ac-ac converter.

The flexibility of an integral-cycle converter may be enhanced if four switches are used in a bridge configuration, as illustrated in Fig. 10.4.1. As before, the load-voltage waveform is constructed using half-cycles from the ac source, but the bridge provides the added ability to reverse the polarity of any half-cycle. In the figure, a resonant *LC* circuit is shown across the input source. It is tuned to the

source frequency to filter out any noise, interference, or distortion which may be present in a practical implementation. This may be necessary since any superimposed noise on the ac source could cause non-zero voltage switching.

EXAMPLE W10.4.2

An integral half-cycle converter, using four switches in a bridge configuration, is illustrated in Fig. 10.4.1. Use this topology to convert an input ac source with a voltage of 500V and a frequency of 5kHz into a load requiring a frequency of roughly 385Hz. Use a resistive load of 10 ohms and assume the source impedance is negligible. In this case it may be assumed that the input source is free of noise and harmonics so that the input *LC* filter is unnecessary. Develop the driver scheme and use PSpice to simulate this circuit. Use PROBE to display the resulting load voltage. Determine **(a)** the total rms and fundamental rms values of the load voltage and **(b)** the total harmonic distortion THD of the load-voltage waveform.

Solution

There are four steps to achieve a solution.

STEP 1

The first step is to transform the circuit diagram into PSpice elements and nodes. The resulting configuration is illustrated in Fig. W10.4.2a.

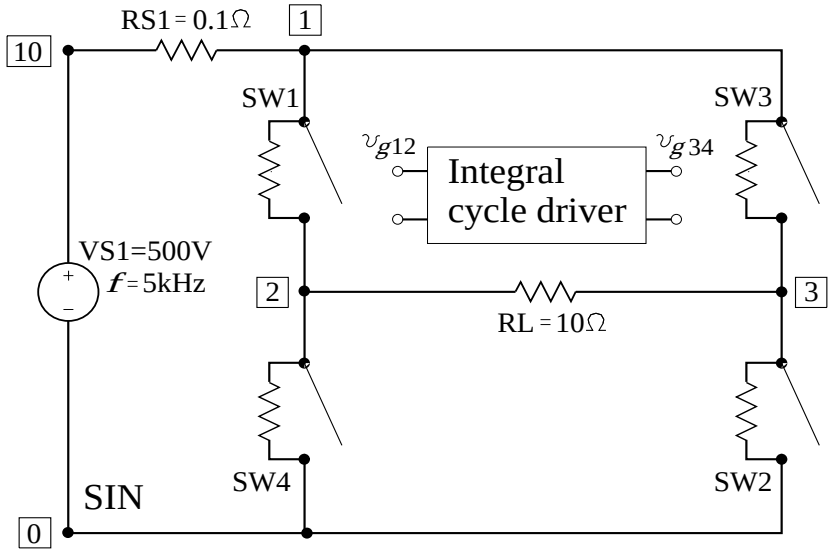

Fig. W10.4.2a Single phase ac-converter configuration.

STEP 2

The next step is to transform the configuration in Fig. W10.4.2a into a PSpice circuit file. The ratio of the input frequency f_s to output frequency f_l is

$f_s/f_l = T_l/T_s = 5000/385 \approx 12.987$.

Since the output waveform must be constructed using some combination of half cycles, the output period must be an integer multiple of the input period. In this case we will round up to an integer multiplier of 13. During each 13 input cycles there are potentially 26 half-cycles which may be used to construct a new alternating waveform close to the required output frequency. A pattern, whereby a sinusoid is approximated by varying the number of clustered half-cycles, is required. One possible switching sequence is illustrated in Fig. W10.4.2b.
In this particular case, with an odd number of input cycles (13) per half cycle of the output voltage, the switches can be bidirectional. In this way, the gate signals have the same pattern each half cycle of the output, but the load-voltage polarity changes each half cycle.
From Fig. W10.4.2b we see that the gate control for this type of converter is quite complex. The controller is required to give an unevenly spaced series of precisely placed pulses. The switch control voltage is not a regular periodic squarewave, so it is best realized in PSpice by using the enhanced piecewise linear source (PWL).

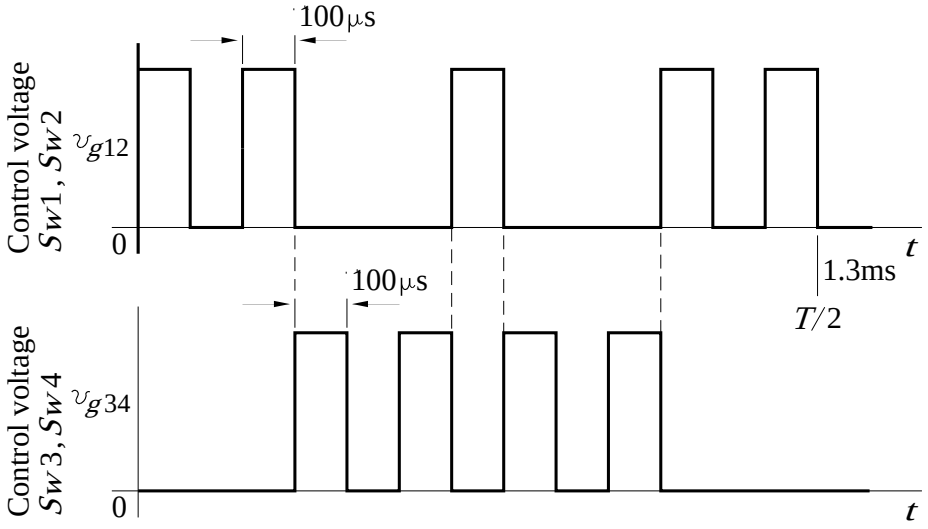

Fig. W10.4.2b Switch control sequence.

» » » » W10_4_2.CIR »

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HIGH-FREQUENCY INTEGRAL HALF-CYCLE AC-AC CYCLOCONVERTER
* The POWER library is used for the switch's model parameters.
.LIB     POWER.LIB
.INC     OPTIONS;                                  Convergence aid.
* PARAMETERS
.PARAM  FREQ=5kHz
.PARAM  RSOURCE=0.1ohm;                            Source resistance.
.PARAM  VRMS=500V  VMAX={SQRT(2)*VRMS}  RLOAD=10ohms
* SOURCE and LOAD
VS   10   0   SIN(0 {VMAX} {FREQ})
RS   10   1   {RSOURCE}
* PWL source driver.
VG12  20    0    PWL   REPEAT  FOREVER
+ 0,1  99.99us,1  100us,0  200us,0  200.01us,1  299.99us,1
+ 300us,0  600us,0  600.01us,1  699.99us,1  700us,0
+ 1000us,0  1000.01us,1  1099.99us,1  1100us,0  1200us,0
+ 1200.01us,1  1300us,1      ENDREPEAT
VG34  21    0    PWL   REPEAT  FOREVER
+ 0,0  300us,0  300.01us,1  399.99us,1  400us,0  500us,0
+ 500.01us,1  599.99us,1  600us,0  700us,0  700.01us,1
+ 799.99us,1  800us,0  900us,0  900.01us,1  999.99us,1
+ 1000us,0  1300us,0   ENDREPEAT
* DEVICES and ELEMENTS.  SWITCH parameters in POWER.LIB
SW1  1   2   20   0   SWITCH
SW2  3   0   20   0   SWITCH
SW3  1   3   21   0   SWITCH
SW4  2   0   21   0   SWITCH
RL   2   3   {RLOAD};                              Output load resistance.
* ANALYSIS
* A time-step ceiling is used to increase the plot resolution.
.FOUR       384.62Hz   15   v(2,3)
.TRAN       5us  3.9ms  0    4us
.PROBE      v(1),       v(2,3);                    Source and load voltages.
.END
```

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STEP 3

The third step is to run the PSpice program with the circuit file W10_4_2.CIR.

STEP 4

The fourth step is to run PROBE and view the results which are displayed in Fig. W10.4.2c.

Part **(a)** of Solution. From PROBE and the file W10_4_2**.**OUT the load voltages are $V_{l\,\mathrm{rms}} = 411.8\mathrm{V}$ and $V_{l1\,\mathrm{rms}} = 281.4\mathrm{V}$.

Part **(b)** of Solution. From the output file W10_4_2**.**OUT, the total harmonic distortion THD of the output-voltage waveform is THD = 88.57%. Compare this with EXAMPLE 10.4.1.

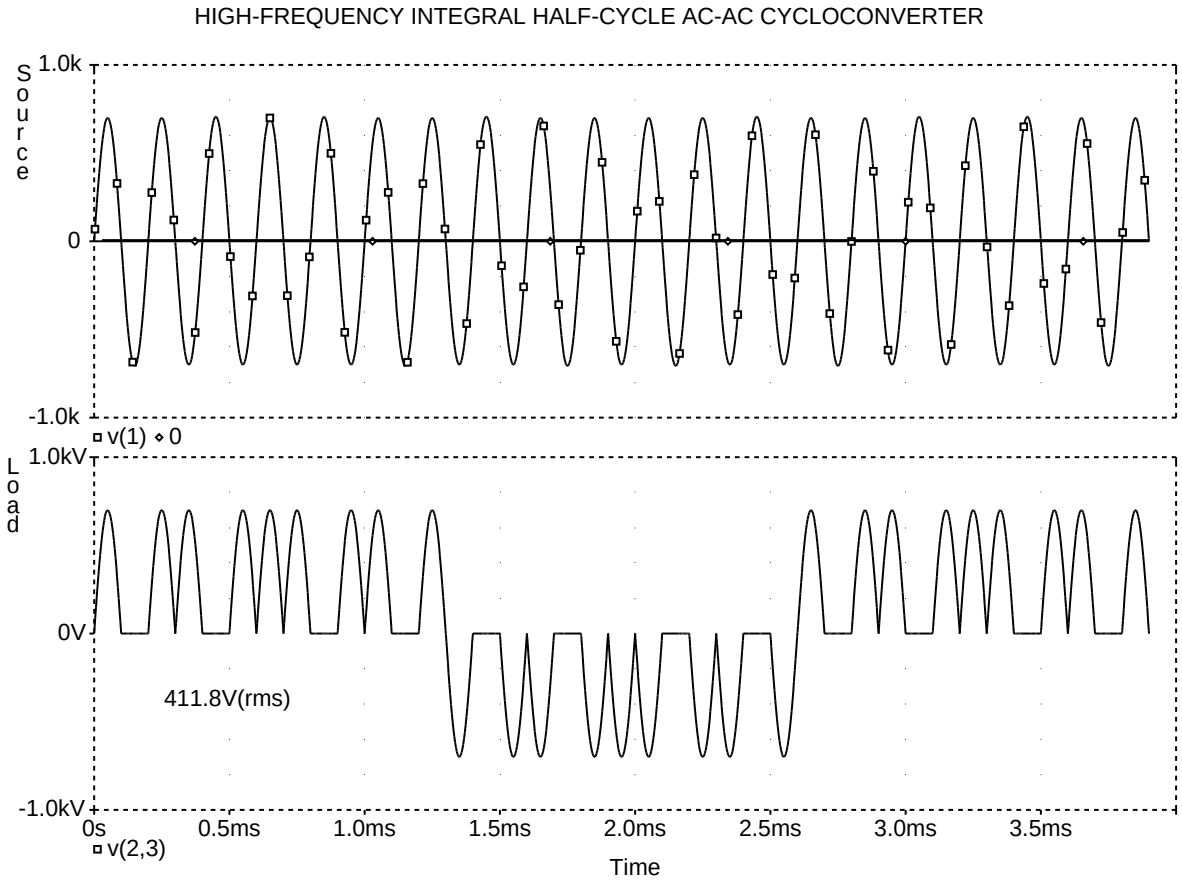

Fig. W10.4.2c

END OF EXAMPLE W10.4.2

Drill Exercise WD10.4.2

Consider EXAMPLE W10.4.2 and modify the circuit file to use a source frequency of 13kHz and an output frequency of 1kHz. Display the load voltage using PROBE. Determine **(a)** the average power absorbed by the load and **(b)** the total harmonic distortion THD of the load-voltage waveform.