

Part 3 of Extra Material for use with

PSpice[®]
Simulation of Power
Electronics Circuits

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See Appendix E in the book.

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9.2.3 SPWM INVERTER DIGITAL DRIVER

What was done in Section 9.2.2 in the text to produce an SPWM inverter with an analogue driver can be done equally well with a digital driver. The following is an example.

EXAMPLE W9.2.1

Consider a centre-tapped source inverter whose circuit diagram is shown in Fig. 9.2.1 in the text. The circuit specifications are as follows.

$V_s = 100\text{V}$, $L_l = 0$, $C_l = 0$, $R_l = 2\Omega$, Sw1 and Sw2 are IGBTs, no diodes, SPWM with a carrier frequency 800Hz, $f = 50\text{Hz}$. Gate voltage 12V.

Do a PSpice simulation using the 555 driver described in EXAMPLE W5.4.1 on the WEB. Plot traces of the gate voltages and the load voltage over one cycle, and plot a load voltage frequency spectrum. Determine (a) the rms value of the load voltage, (b) the average power absorbed by the load and (c) the total harmonic distortion THD of the load-voltage waveform.

Solution

We can use the digital SPWM driver from EXAMPLE W5.4.1 to trigger the switches of the power circuit in EXAMPLE 9.2.1 in the text. A little analogue interfacing is needed.

There are four steps in the solution.

STEP 1

From the PSpice configurations in Fig. W5.4.1a and Fig. EX9.2.1a in the text a PSpice configuration for this example can be drawn. It is shown in Fig. W9.2.1a.

STEP 2

The circuit file named W9_2_1.CIR can be written by using the configuration in Fig. W9.2.1a.

For a given value of the 555 timer capacitor $C = 0.1\mu\text{F} \equiv \text{CAPT}$, a maximum value of $v_s = 10\text{V} \equiv \text{VHI}$ (for the maximum pulse width) and a carrier frequency $f_C = 800\text{Hz} \equiv \{\text{FREQC}\}$ the value of the timer resistance $R \equiv \text{RT}$ is given by eq. (5.4.6) to be

$$\text{RT} = \{1/(\text{FREQC} * \text{CAPT} * \log(\text{VCC}/(\text{VCC} - \text{VHI})))\}$$

The output frequency f of the inverter is to be 50Hz. Thus, the sinusoidal reference signal is to have a frequency $f_{\text{ref}} = 2f = 100\text{Hz}$.

No value is given for the amplitude of the reference signal, so the choice is ours. We will choose the value given in EXAMPLE W5.4.1. The timer's power supply is $\text{VCC} = 12\text{V}$. The minimum value of the reference signal is greater than zero (assume 2V). The maximum value of the reference signal is less than VCC (assume 10V). Let the carrier pulse width at the timer input be as short as $10\mu\text{s}$.

The gate signals to SW1 have to be enabled over only the first half of the inverter-output period. A dependent source EG1 is used for this. The gate signals to SW2 have to be enabled over only the second half of the inverter-output period. A dependent source EG2 is used for this.

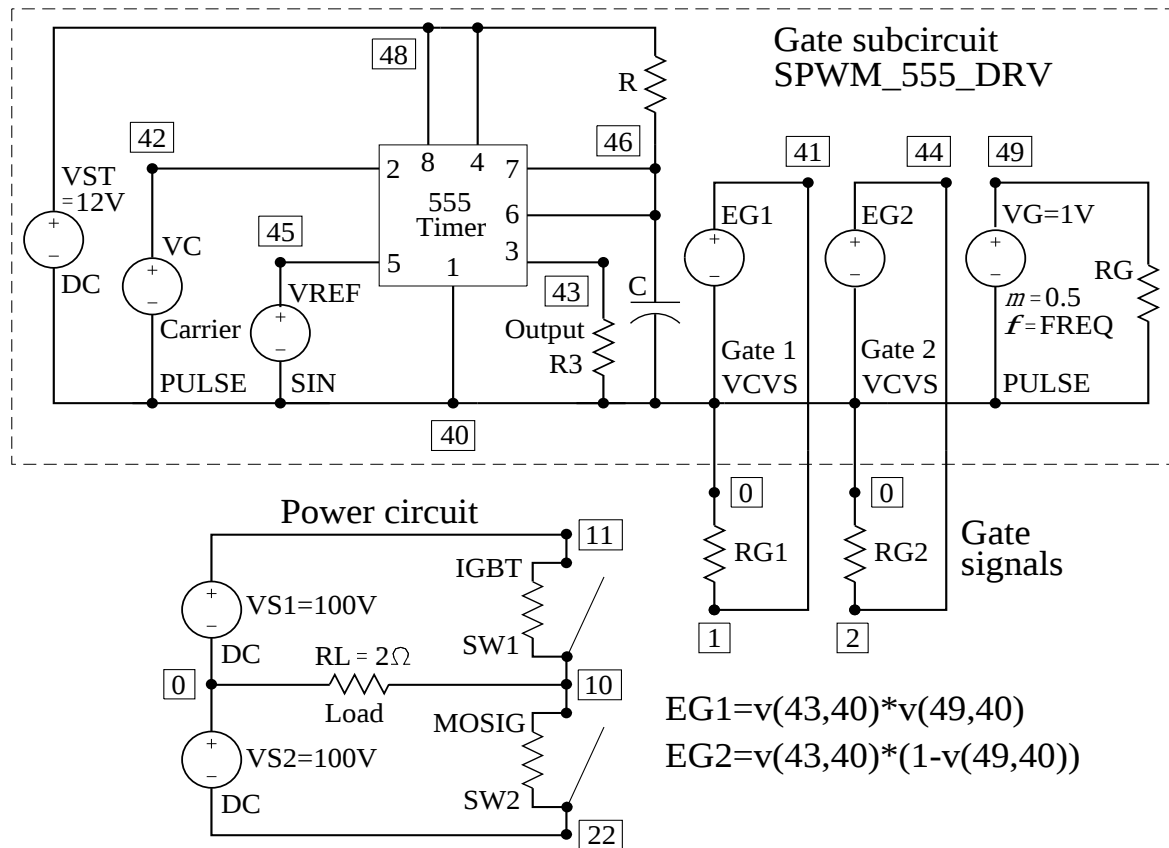


Fig. W9.2.1a Inverter configuration with 555 timer.

[illegible]

SPWM INVERTER WITH A 555 DRIVER

* To determine the output responses.

```
.INC  OPTIONS;
```

Convergence aid.

* PARAMETERS of the driver.

```
.PARAM VCC=12V; The gate signal magnitude and the 555 voltage source.
```

```
.PARAM    TON=10us;           Carrier pulse width.
```

```
.PARAM    TR=10ns TF={TR};
```

Rise and fall times of gate pulse.

```
.PARAM    FREQ=50Hz PERIOD={1/FREQ}; Inverter frequency.
```

```
.PARAM FREQREF={2*FREQ};           Reference frequency.
```

```
.PARAM    NUM=8;           Pulses per half cycle of inverter.
```

```
.PARAM FREQC={NUM*FREQREF}; Carrier frequency.
```

```
.PARAM PER={1/FREQC}; Period of carrier signals.
.PARAM VHI=10V VLO=2V; Range of reference voltage.
.PARAM VDC={VHI/2+VLO/2}; DC offset reference voltage.
.PARAM VMAX={VHI/2-VLO/2}; Amplitude of reference voltage.
.PARAM DEL=-90deg; Reference delay to start short pulses.
.PARAM CAPT=0.1uF; Timer external capacitor.
.PARAM RAT={VCC/(VCC-VHI)}; Equation (5.4.6).
.PARAM RT={1/(FREQC*CAPT*log(RAT))}; Timer external resistor.
* PARAMETERS of the power circuit.
.PARAM VS=100V; The sources VS1 and VS2.
.PARAM RLOAD=2ohms; The load resistance.

* DRIVER SUBCIRCUIT, see EXAMPLE W5.4.1 and Fig. W9.2.1a.
.SUBCKT SPWM_555_DRV 40 41 44
* SOURCES
VST 48 40 DC {VCC}; Timer source.
VC 42 40 PULSE({VCC} 0 10ns {TR} {TF} {TON} {PER}); Carrier.
VREF 45 40 SIN({VDC} {VMAX} {FREQREF} 0 0 {DEL})
VG 49 40 PULSE(0 1 0 {TR} {TF} {PERIOD/2-2*TR} {PERIOD})
* VG directs the gate signals to the switches Sw1 and Sw2.
EG1 41 40 VALUE={v(49,40)*v(43,40)}; Gate 1 signal source.
EG2 44 40 VALUE={{(1-v(49,40))*v(43,40)}}; Gate 2 signal source.
* CIRCUIT ELEMENTS
R3 43 40 1E5; Nominal load for timer output.
R 48 46 {RT}; Timer resistance.
C 46 40 {CAPT}; Timer capacitor.
RG 49 40 1E5; Nominal load for VG.
Xtimer 40 42 43 48 45 46 46 48 555D; Calls 555 timer.
.ENDS SPWM_555_DRV

.LIB EVAL.LIB

* SOURCES of the power circuit.
VS1 11 0 DC {VS}
VS2 0 22 DC {VS}

* LOADS
RL 10 0 {RLOAD}
RG1 1 0 1E5; Equivalent gate resistance.
RG2 2 0 1E5

* SUBCIRCUIT for IGBT model, a voltage-controlled switch.
.SUBCKT IG_IDEAL 11 10 1 32; Drain, source, gate pair.
SW 11 10 1 32 MOSIG; Voltage-controlled switch.
.MODEL MOSIG VSWITCH(RON=1E-3 ROFF=1E6
+ VON=10 VOFF=1E-3)
.ENDS IG IDEAL
```

Fig. W9.2.1b

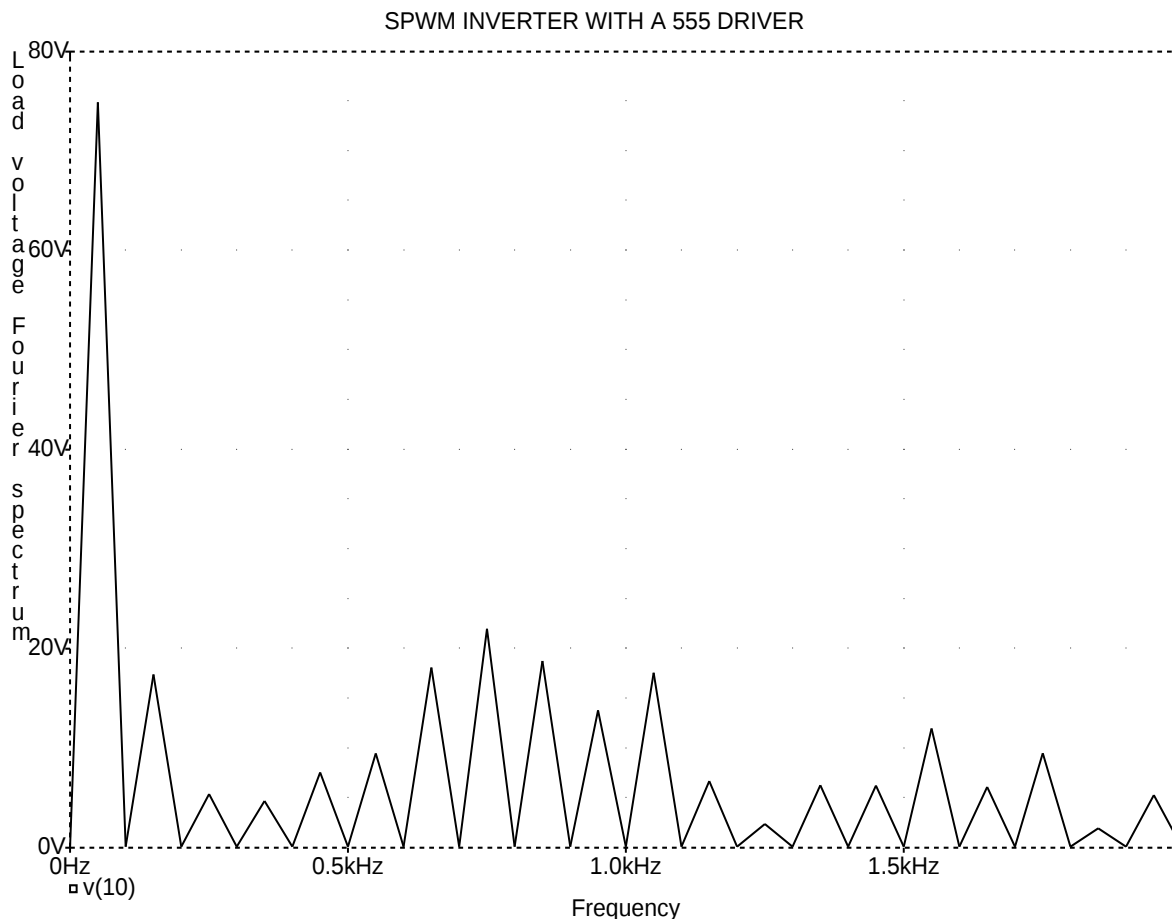


Fig. W9.2.1c

The Fourier spectrum of the load-voltage waveform is plotted in Fig. W9.2.1c. The trace is obtained by clicking on **X_axis** in the main menu of PROBE. Then the cursor can be clicked on **Fourier** in the submenu. Clicking on **X_axis** again enables us to click on **Set_scale**, then type in 0,2kHz and hit <ENTER>. We then escape to the main menu and add the load voltage v(10) as a new trace. The spectrum trace joining the amplitude of each harmonic appears on the screen.

Part (a) of Solution. From the trace of load voltage, the periodic rms value is $V_{l_{rms}} = 67.67V$.

Part (b) of Solution. The average power absorbed by the load is given by

$$P = V_{l_{rms}}^2 / R_l = 67.67^2 / 2 \approx 2.29kW.$$

Part (c) of Solution. From the results of the Fourier analysis in W9_2_1.OUT the total harmonic distortion is $\text{THD} = 48.58\%$.

The 555 gate driver with the interface for a single-phase SPWM inverter has been written as a subcircuit in this circuit file. For easy access this subcircuit has been named SPWM_555_DRV and written to DRIVER.LIB.

END OF EXAMPLE W9.2.1

Drill Exercise WD9.2.1

Consider the centre-tapped source inverter whose circuit diagram is shown in Fig. 9.2.1 in the text. The inverter is to have a sinewave pulse-width modulated (SPWM) output. The circuit has the following specifications.

$V_s = 100\text{V}$, $L_l = 0$, $C_l = 0$, $R_l = 3\Omega$, SPWM driver,

$f = 60\text{Hz}$. Ten-pulse output per half cycle. Gate voltage 15V.

Use the power circuit from EXAMPLE 9.2.1 in the text. Use the driver subcircuit named SPWM_555_DRV in DRIVER.LIB with the following specifications.

$V_{CC} = 12\text{V}$, 555 reference signal 9V(max), 3V(min) for inverter voltage control.

Do a PSpice simulation and plot traces of the gate voltages and the load voltage, and plot the Fourier spectrum of the load voltage. Determine **(a)** the rms value of the load voltage, **(b)** the average power absorbed by the load and **(c)** the total harmonic distortion THD of the output-voltage waveform.

(Ans: **(a)** 73.88V, **(b)** 1.82kW, **(c)** 19.15%.)

9.3.1 UNIFORM MULTIPLE-PULSE INVERTER

Multiple pulses in each half cycle of an inverter output give control over both the harmonic content and the rms value of the voltage across a load. See Fig. 9.2.2. Both the duty cycle and the number of pulses are variables and both are controlled by the gate signals to the inverter switches. We can adapt and expand the gate drive circuits that were described in Chapter 5 and in Section 9.2.1 for the single-phase, bridge inverter, depicted in Fig. 9.3.1 in the text. View the subcircuit MPLS_TRI_INV in DRIVER.LIB.

EXAMPLE W9.3.1

A single-phase, bridge inverter is illustrated in Fig. 9.3.1 in the text. The main circuit specifications are as follows for multiple-pulse operation.

$V_s = 100\text{V}$, $L_l = 10\text{mH}$, $R_l = 5\Omega$, IGBT switches, diodes connected, $m = 0.4$, $f = 50\text{Hz}$. Three-pulse output per half cycle. Gate voltage 15V.

The gate driver is to be simulated by a triangular wave signal, a reference signal and a comparator, similar to the driver described in EXAMPLE 5.2.2 in the text. Do a PSpice simulation and plot traces of the source current i_s , a gate voltage waveform and the load voltage and current for steady conditions. Determine **(a)** the average power delivered by the source, **(b)** the total harmonic distortion THD of the load-voltage and current waveforms and **(c)** the peak value of the load current.

Solution

This example is an exercise to produce a suitable driver that generates uniform gate pulses at a frequency of 300Hz, each pulse with a duty cycle of 0.4, $m = t'_{ON}/(2T')$. See Fig. W9.3.1a. If the carrier v_C and reference v_{ref} signals are the inputs of a comparator, then output pulses are finite if $v_{ref} > v_C$. These pulses can be applied in groups of three alternately to each pair of switches Sw1, Sw2 and Sw3, Sw4. The output frequency of the inverter is $f_c/6$ where f_c is the carrier signal frequency.

The solution is achieved in four steps.

STEP 1

From the circuit diagram in Fig. 9.3.1 in the text, from the given specifications, from EXAMPLE 5.2.2 in the text, and from the diagrams in Fig. W9.3.1a the PSpice configuration can be drawn.

This is shown in Fig. W9.3.1b.

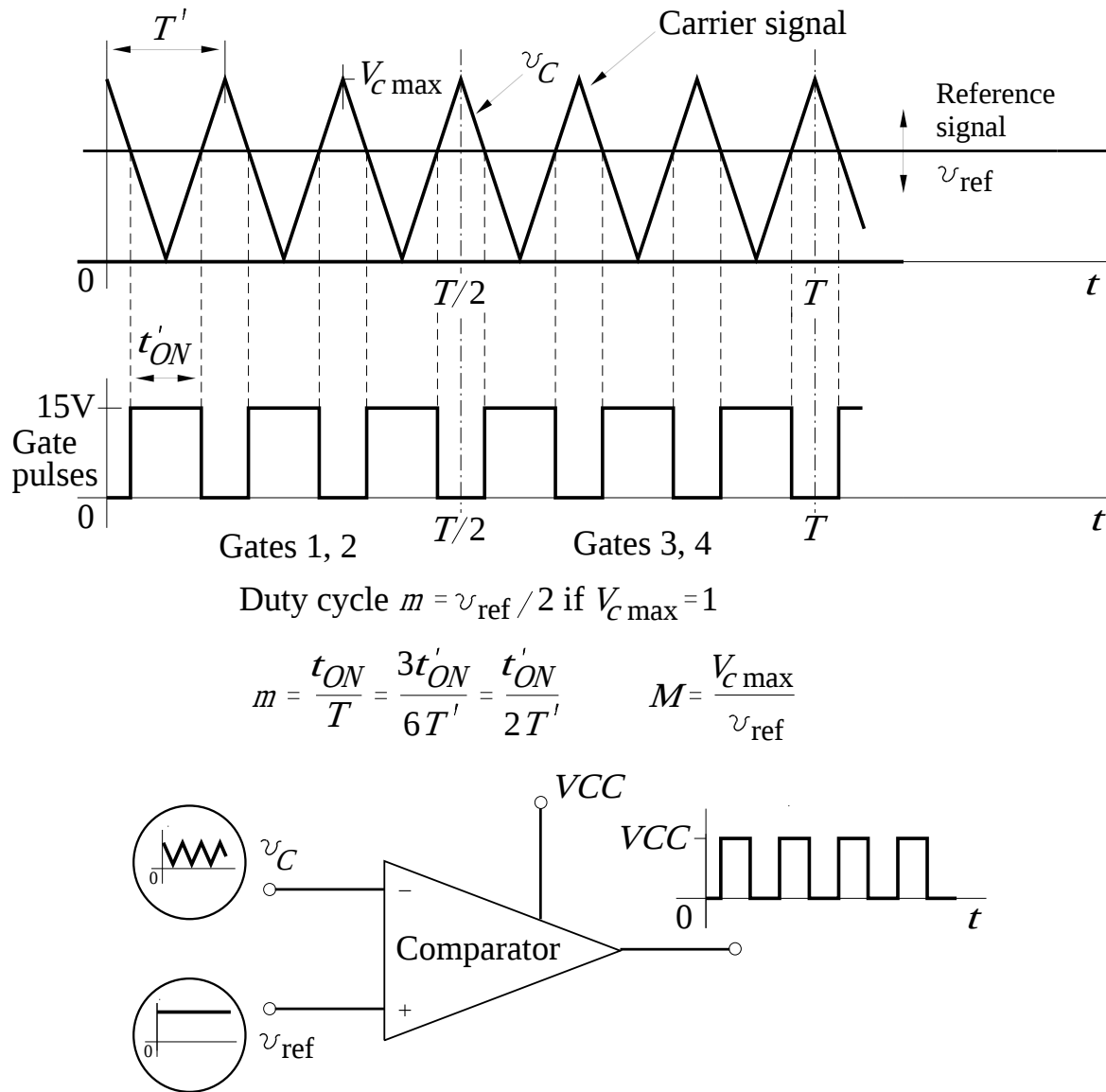


Fig. W9.3.1a Gate pulse formation.

STEP 2

From the PSpice configuration in Fig. W9.3.1b, a circuit file can be written. The circuit file is called W9_3_1.CIR.

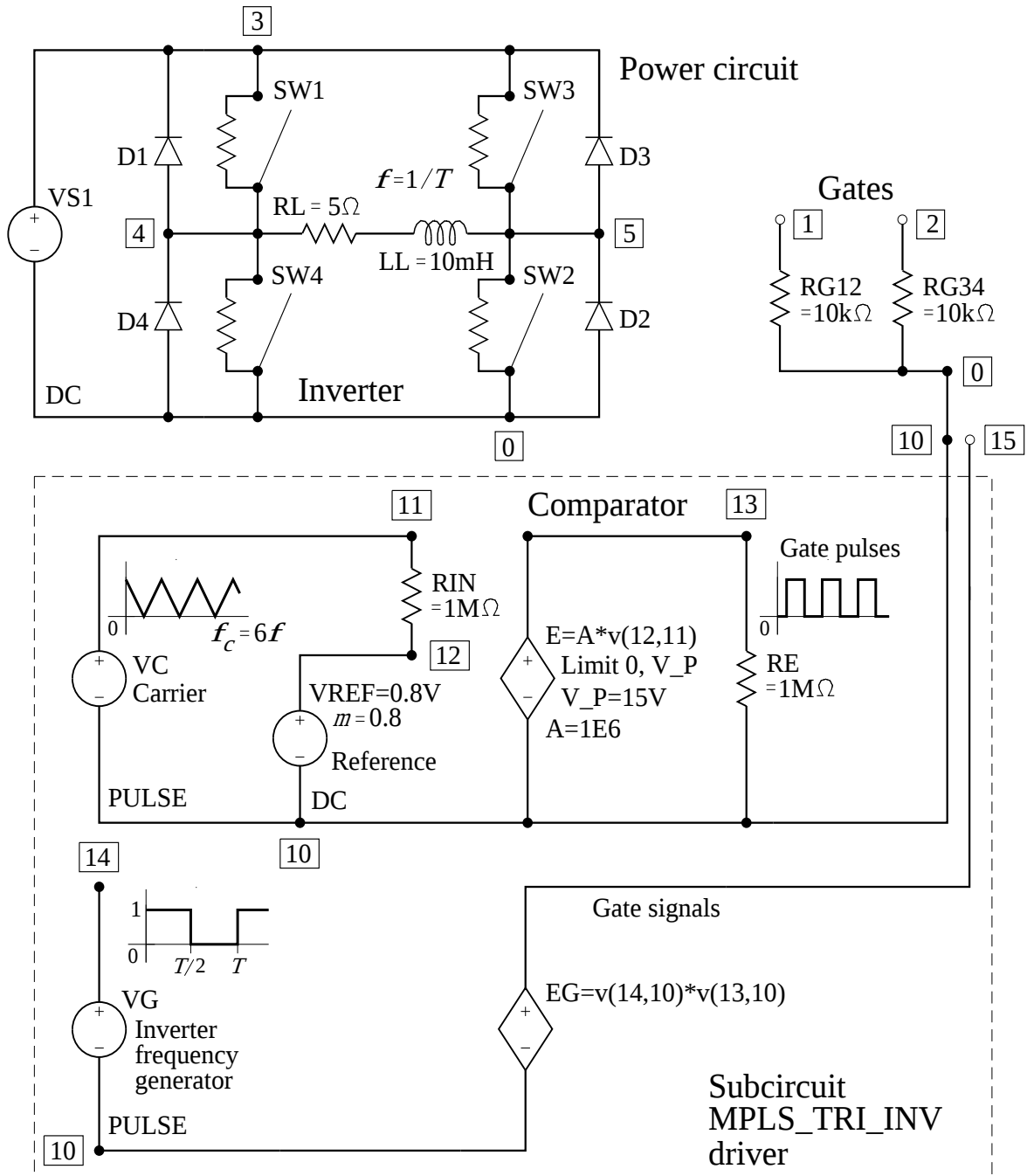


Fig. W9.3.1b Multiple-pulse configuration.

STEP 3

A PSpice simulation can be run with the circuit file W9_3_1.CIR. The results will be written in W9_3_1.OUT and W9_3_1.DAT.

* To determine power and harmonic distortion.

.INC OPTIONS; An OPTIONS file for convergence stability.

.PARAM	VS=100V;	Source voltage.
.PARAM	RLOAD=5ohms;	Load resistance.
.PARAM	LLOAD=10mH;	Load inductance.
.PARAM	FREQ=50Hz PERIOD={1/FREQ};	Inverter output frequency.
.PARAM	TR=20ns TF={TR};	Pulse rise and fall times.
.PARAM	DUTY=0.4;	Duty cycle $m = t_{ON} / T$.
.PARAM	TON={PERIOD/2 - 2*TR};	On-time of frequency generator.
.PARAM	VP=15V;	Magnitude of gate voltage.
.PARAM	NUM=3;	Pulse number per half cycle.
.PARAM	PER={0.5*PERIOD/NUM};	Period of pulses and carrier signals.
.PARAM	VC=1V;	Carrier pulse magnitude.
.PARAM	VREF={2*DUTY*VC};	Reference voltage.
.PARAM	DELC={TR/2};	Delay of carrier pulse.
.PARAM	TRC={PER/2 - TR};	Rise time of carrier pulse.
.PARAM	TFC={TRC};	Fall time of carrier pulse.
.PARAM	WID={TR};	Carrier pulse on-time.
.PARAM	DEL={PERIOD/2};	Delay for frequency generator pulse.

VS1	3	0	DC	{VS}	
RL	4	55		{RLOAD}	
LL	55	5		{LLOAD}	IC=-9.93A; See trace.
RG12	1	0	1E4;		Gate resistance of Sw1 and Sw2.
RG34	2	0	1E4		

```
.SUBCKT IG_IDEAL 17 18 19 20; Drain(17). Source(18). Gate(19,20).
SW 17 18 19 20 MOSIG; Voltage-controlled switch.
.MODEL MOSIG VSWITCH(ROFF=1E6 VON=10 VOFF=1E-3)
.ENDS IG_IDEAL
.SUBCKT D_IDEAL 21 22; Anode(21).
DIO 21 22 DIODE
.MODEL DIODE D(RS=1m CJO=0.1pF N=0.001)
.ENDS D_IDEAL
```

XSW1	3	4	1	0	IG_IDEAL;	Switch Sw1.
XSW2	5	0	1	0	IG_IDEAL;	Switch Sw2.
XSW3	3	5	2	0	IG_IDEAL;	Switch Sw3.
XSW4	4	0	2	0	IG_IDEAL;	Switch Sw4.
XD1	4	3			D_IDEAL;	Diode D_1 .
XD2	0	5			D_IDEAL;	Diode D_2 .

```

XD3      5   3   D_IDEAL;           Diode D3.
XD4      0   4   D_IDEAL;           Diode D4.

* SUBCIRCUIT for IGBT driver.
.SUBCKT MPLS_TRI_INV 15 10 PARAMS: DELAY=0
* The carrier-wave source.
VCAR 11 10 PULSE({VC} 0 {DELC} {TRC} {TFC} {WID} {PER})
VR    12 10 DC {VREF};              Reference voltage source.
* Comparator output, voltage is clipped between zero and VP.
E     13 10 VALUE={LIMIT(v(12,11)*1E6, 0, VP)}
RE    13 10 1E6
* Frequency generator VG for the inverter.
VG    14 10 PULSE(0 1 {DELAY} {TR} {TF} {TON} {PERIOD})
* Gate pulse generator.
EG    15 10 VALUE={v(14,10)*v(13,10)}; Pulses in a half cycle.
.ENDS MPLS_TRI_INV
* MPLS (Multiple pulse), TRI (TRIangular wave), INV (INVerter).
* CALLS for gate drivers.
Xdriver1 1 0 MPLS_TRI_INV
Xdriver2 2 0 MPLS_TRI_INV PARAMS: DELAY={DEL}

* ANALYSIS
* .TRAN 40us 80ms UIC; To find initial conditions for LL in steady state.
.TRAN 40us 40ms UIC
.FOUR 50Hz 15 v(4,5) i(RL)
.PROBE i(VS1), v(4,5), i(RL), v(1)
.END

```

STEP 4

STEP 4 Using PROBE, traces can be plotted for the source current the load voltage, a gate-driver waveform and the load current. See Fig. W9.3.1c. These waveforms are less than ideal because of the slew rate in the output of the comparator. The slew rate is caused by numerical stability and large step sizes in the analysis.

Part (a) of Solution. From the source-current trace, the average value of the source current is $I_{s,av} = 5.49\text{A}$. Thus, the average power P delivered by the source is

$$P = V_s I_{s_{av}} = 100 \times 5.49 = 549 \text{ W.}$$

Part (b) of Solution. From the file W9_3_1.OUT, the output-waveform distortion is given as follows.

For the load voltage, THD=125.9%. For the load current, THD=42.7%.

Part (c) of Solution. From the trace of the load current in Fig. W9.3.1c the peak value is $I_{l\max} = 15.1\text{A}$.

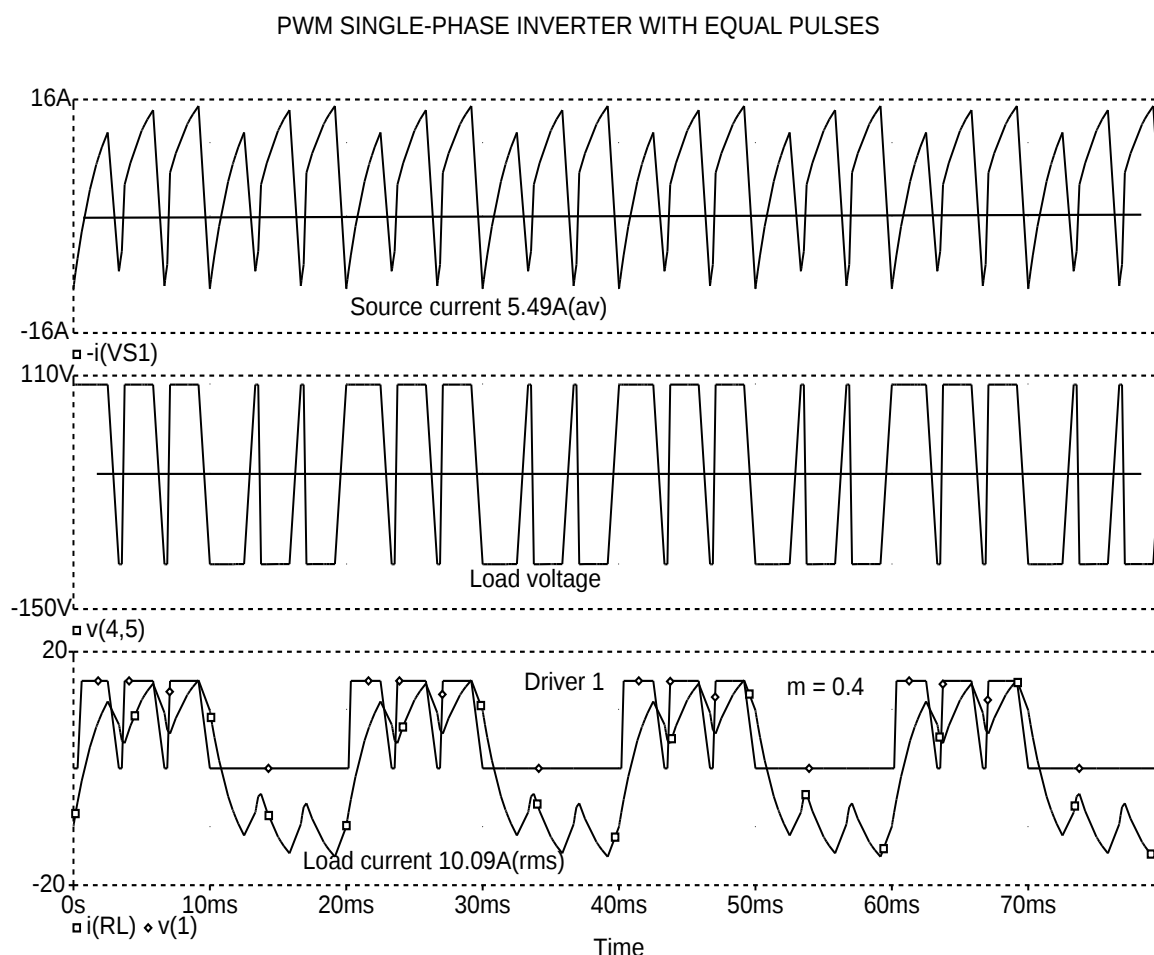


Fig. W9.3.1c

END OF EXAMPLE W9.3.1

Drill Exercise WD9.3.1

A single-phase, bridge inverter is illustrated in Fig. 9.3.1 in the text. The circuit has the following specifications.

$V_s = 200\text{V}$, $L_l = 0$, $R_l = 10\Omega$, IGBT switches, $m = 0.3$, $f = 100\text{Hz}$.

Two-pulse output per half cycle. Gate voltage 15V.

Use the PWM gate driver INV_MLT_PLS, described in DRIVER.LIB and Drill Exercise D9.2.3 in the text, or gate driver MPLS_TRI_INV described in EXAMPLE W9.3.1 and do a PSpice simulation. Plot traces of the dc source current and the load current. Determine **(a)** the average power delivered to the load and **(b)** the total harmonic distortion THD of the load-current waveform.

(Ans: **(a)** 2.4kW, **(b)** 85.65%.)

Drill Exercise WD9.3.2

Consider the circuit diagram of a single-phase, bridge inverter in Fig. 9.3.1 in the text. The circuit has the following specifications.

$$V_s = 48\text{V}, L_l = 0, R_l = 1\Omega, \text{ IGBT switches, } m = 0.3, f = 100\text{Hz}.$$

Four-pulse output per half cycle. Gate voltage 12V.

Adapt the 555-timer driver in EXAMPLE W9.2.1 (on the WEB in Section 9.2.3) to give uniform pulsewidth PWM using a dc reference voltage. Name the driver subcircuit PWM_555_DRV. Do a PSpice simulation and plot traces of the source current and output current over four cycles. Determine **(a)** the total harmonic distortion THD of the load-current waveform, **(b)** the fundamental rms value of the load current and **(c)** the average power delivered to the load.

(Ans: **(a)** 91.61%, **(b)** 36.98A, **(c)** 1.37kW.)

9.3.3 CURRENT-SOURCE INVERTER

Current-source inverters (CSI) are used to drive induction motors. Figure 9.3.2 shows a simplified circuit diagram of a single-phase, bridge CSI together with the gate-signal waveforms and the load-current waveform.

The dc supply is represented by a constant-current source. In practice this is an adjustable voltage source in series with an inductor of large value.

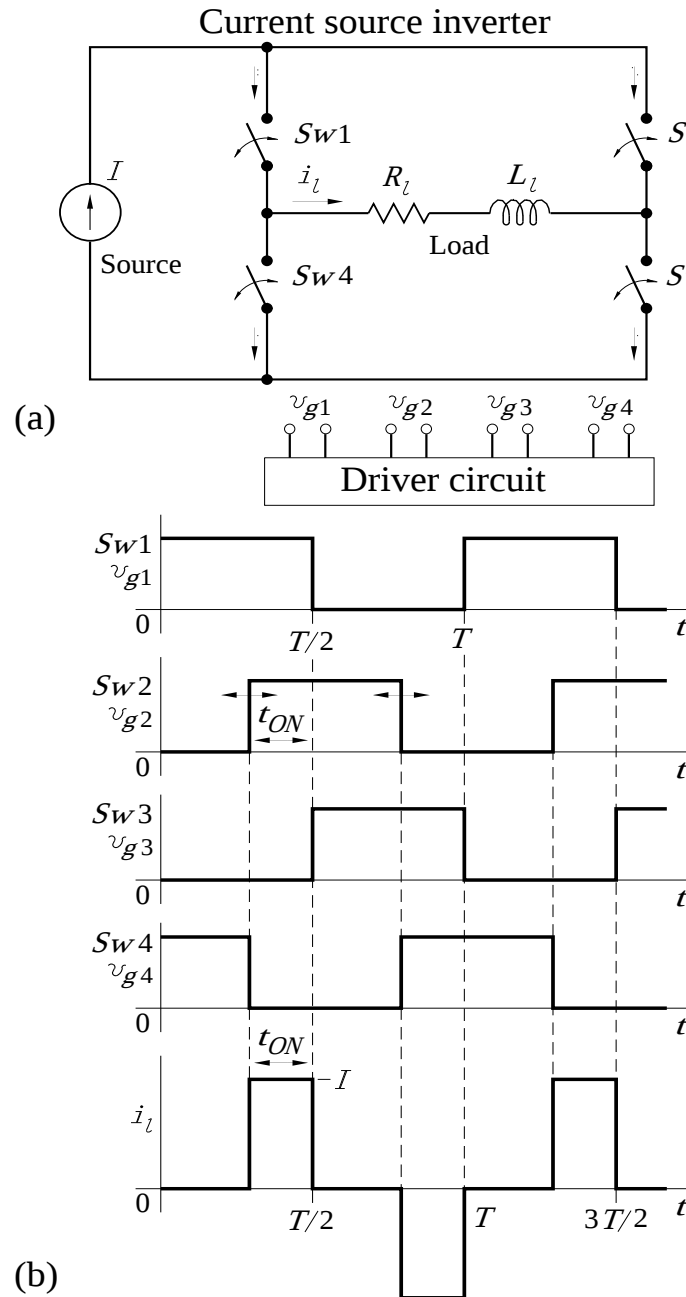


Fig. 9.3.2 Current-source inverter.
(a) Circuit diagram, (b) waveforms.

The four switches of the inverter must provide a closed path for the source current at all times. One strategy is to have two switches on at any time. For example, we have the choice of pairs Sw1, Sw2, or Sw1, Sw4, or Sw3, Sw4, or Sw3, Sw2. A possible sequence of pair switching is Sw1 and Sw2, Sw2 and Sw3, Sw3 and Sw4, Sw4 and Sw1 with the cycle repeating. Between each pair of switching operations there must be overlap in order that the source current has a closed path. This is arranged in the gate-driver design.

For this particular strategy the frequency of the inverter output is determined by the switching frequency of the gate signals. The rms value of the load current can be controlled by both the magnitude of the source current and the common time t_{ON} that the appropriate switch pairs, Sw1, Sw2 and Sw3, Sw4 are on. See Fig. 9.3.2b.

EXAMPLE W9.3.2

Consider the current-source inverter depicted in Fig. 9.3.2. The circuit has the following specifications.

$$I = 50\text{A}, L_l = 0, R_l = 2\Omega, f = 50\text{Hz}, \text{ duty cycle } m = 0.3.$$

$$(m = t_{ON}/T, 0 \leq m \leq 0.5).$$

Model the switches by PSpice voltage-controlled switches and do a simulation. Plot traces of the load current, the product of the signals v_{g1} and v_{g2} and the source voltage. Determine **(a)** the average power delivered by the source and **(b)** the total harmonic distortion THD of the load-voltage waveform.

Solution

We can carry out the solution in four steps. Note that the gate signals in Fig. 9.3.2 are similar to those described in Drill Exercise D9.3.2 in the text.

STEP 1

From the example data and from Fig. 9.3.2, we can draw a PSpice configuration of the inverter. This is shown in Fig. W9.3.2a.

STEP 2

From the example data and from the PSpice configuration in Fig. W9.3.2a, a circuit file can be written. The circuit file is called W9_3_2.CIR. Since the switches are not unidirectional there can be load current freewheeling during the switching transitions if the load is inductive. Series diodes would prevent freewheeling.

I	0	5	DC {IS};	The dc power supply.
RL	6	7	{RLOAD}	

* SUBCIRCUITS for the SWITCHES

```
.SUBCKT IG_IDEAL 17 18 19 20; From EXAMPLE 9.3.3 (text).
SW 17 18 19 20 MOSIG;          Voltage-controlled switch.
.MODEL MOSIG VSWITCH(ROFF=1E-3 ROFF=1E6 VON=10 VOFF=1E-3)
.ENDS IG_IDEAL
```

* CALLS for the FOUR SWITCHES of the INVERTER.

XSW1	5	6	1	0	IG_IDEAL;	Switch Sw1.
XSW2	7	0	2	0	IG_IDEAL;	Switch Sw2.
XSW3	5	7	3	0	IG_IDEAL;	Switch Sw3.
XSW4	6	0	4	0	IG_IDEAL;	Switch Sw4.

* DRIVER circuits.

VG1	1	0	PULSE({VP} 0 {DEL1} {TR} {TF} {PW1} {PERIOD})
VG2	2	0	PULSE(0 {VP} {DEL2} {TR} {TF} {PW2} {PERIOD})
VG3	3	0	PULSE({VP} 0 {DEL3} {TR} {TF} {PW3} {PERIOD})
VG4	4	0	PULSE({VP} 0 {DEL4} {TR} {TF} {PW4} {PERIOD})
RG1	1	0	50; Gate resistance.
RG2	2	0	50
RG3	3	0	50
RG4	4	0	50

* ANALYSIS

```

. TRAN      40us  20ms    UIC
. FOUR      50Hz  15      v(6,7)
. PROBE      v(5), v(6,7), v(1), v(2)
. END

```

[illegible]

STEP 3

A PSpice simulation can be run with the circuit file W9_3_2.CIR.

STEP 4

Using PROBE with the data file W9_3_2.DAT, traces of the load voltage, a common gate pulse and the source voltage can be plotted. See Fig. W9.3.2b.

Part (a) of Solution. The average power P delivered by the source is, from the plot, $P = IV_{s_{av}} = 50 \times 60.1 = 3005 \text{ W}$.

Part (b) of Solution. From the output file W9_3_2.OUT, the total harmonic distortion THD of the output-voltage waveform can be obtained. It is $\text{THD} = 33.37\%$.

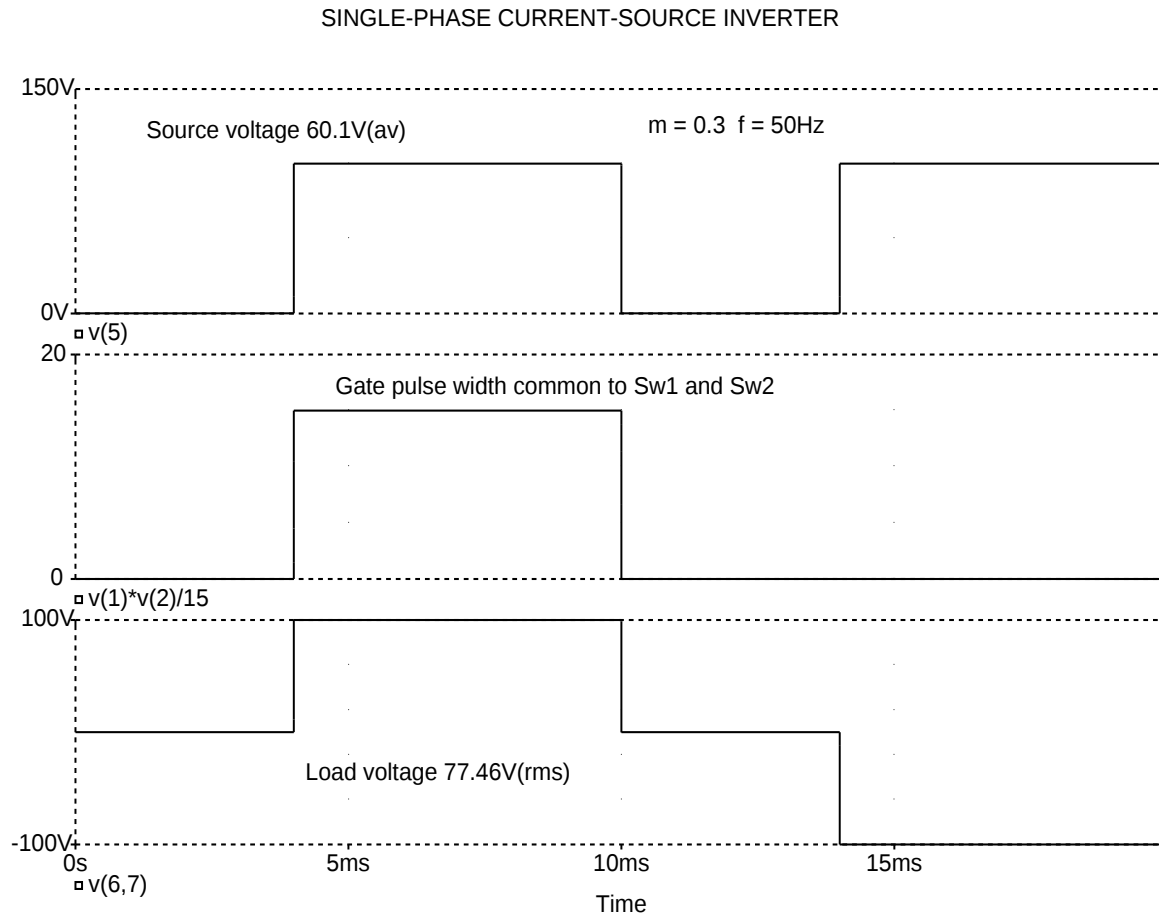


Fig. W9.3.2b

END OF EXAMPLE W9.3.2

9.3.4 CYCLOCONVERTER

A cycloconverter is an ac-ac converter, converting an ac supply of one frequency to an ac source of another frequency at the load, with or without voltage adjustment.

Figure 9.3.3a depicts two single-phase rectifiers that are connected back-to-back. The converter P provides the positive half cycles of voltage to the load while converter N is off. The negative half cycles of voltage appear across the load if converter N is on while converter P is inactive. This configuration sets a load frequency to be a fraction of the source frequency. The fraction depends on the number of half cycles of the supply conducted by each rectifier. That is, $f_o = f/n$, where f is the supply frequency, n is the number of rectifier half cycles in a sequence and f_o is the load frequency of alternation.

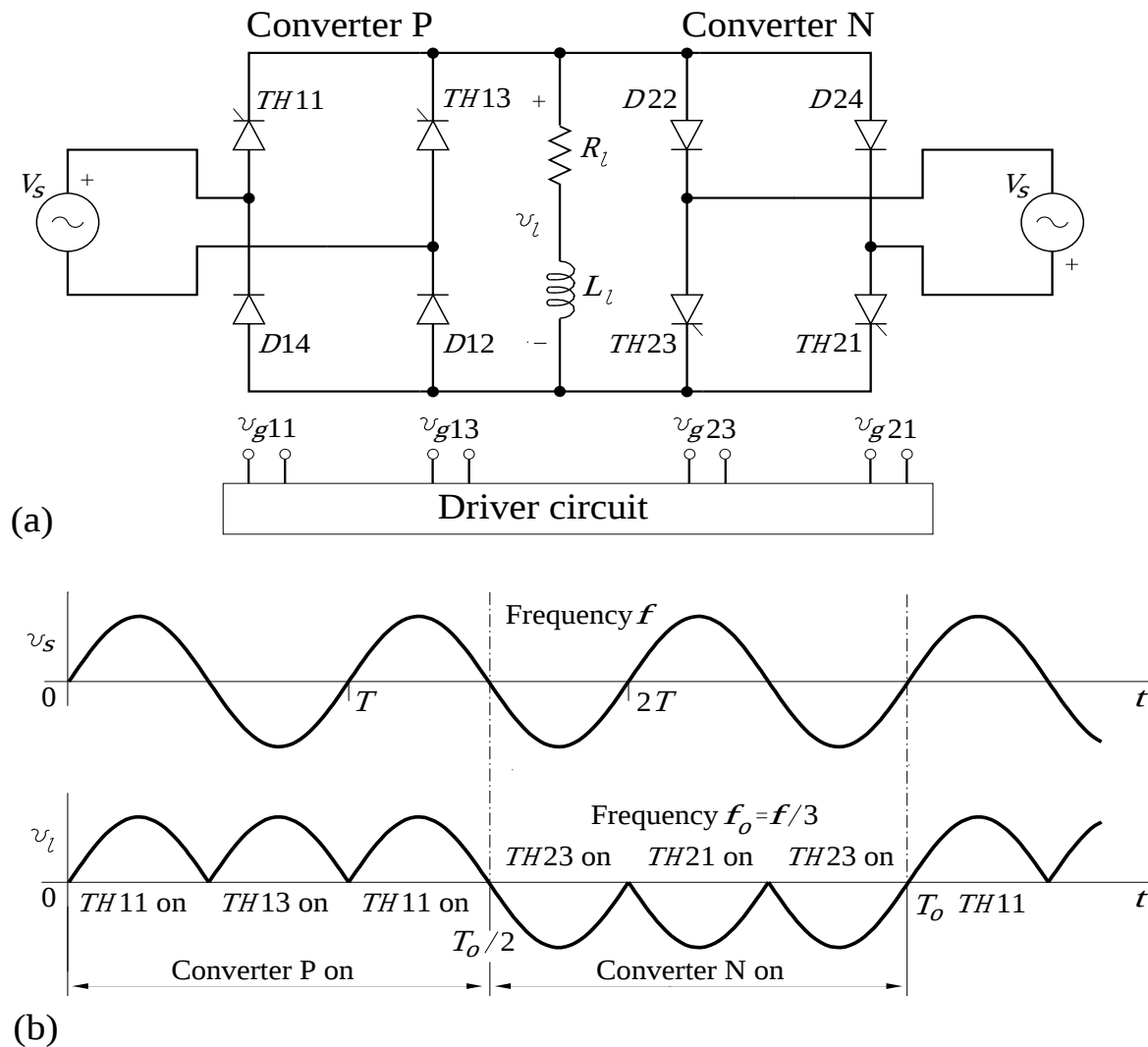


Fig. 9.3.3 Single-phase cycloconverter.
(a) Circuit diagram, (b) waveforms.

Figure 9.3.3b shows possible waveforms. The harmonic content of the output voltage is high. Control of the rms voltage of the output is achieved by phase angle α adjustment. Modulation of α over each output half cycle of voltage will tend to reduce the harmonic content.

EXAMPLE W9.3.3

Consider the single-phase cycloconverter illustrated in Fig. 9.3.3. The circuit has the following specifications.

$$V_s = 120\text{V(rms)} \text{ at } 150\text{Hz}, L_l = 0, R_l = 10\Omega, \\ \text{output frequency } f_o = 50\text{Hz}, \text{ delay angle } \alpha = 0.$$

Do a PSpice simulation and plot traces of the supply voltage and the load current. Determine **(a)** the average power absorbed by the load, **(b)** the total harmonic distortion THD of the load-current waveform, **(c)** the fundamental rms value of the load current and **(d)** the harmonic factors HF of the third, fifth, seventh and ninth harmonics of the load-current waveform.

Solution

There are four steps to achieve a solution.

STEP 1

From the data and from Fig. 9.3.3, we can draw a PSpice configuration to suit the cycloconverter. See Fig. W9.3.3a. Since the load is resistive the thyristors can be modelled by a PSpice voltage-controlled switch with the control voltage (gate signal) being applied as long as conduction is required.

STEP 2

From Fig. 9.3.3 and Fig. W9.3.3a a circuit file can be written. Here, it is named W9_3_3.CIR. It is left as an exercise to interpret the statements of this circuit file.

STEP 3

A PSpice simulation can be run with the circuit file W9_3_3.CIR.

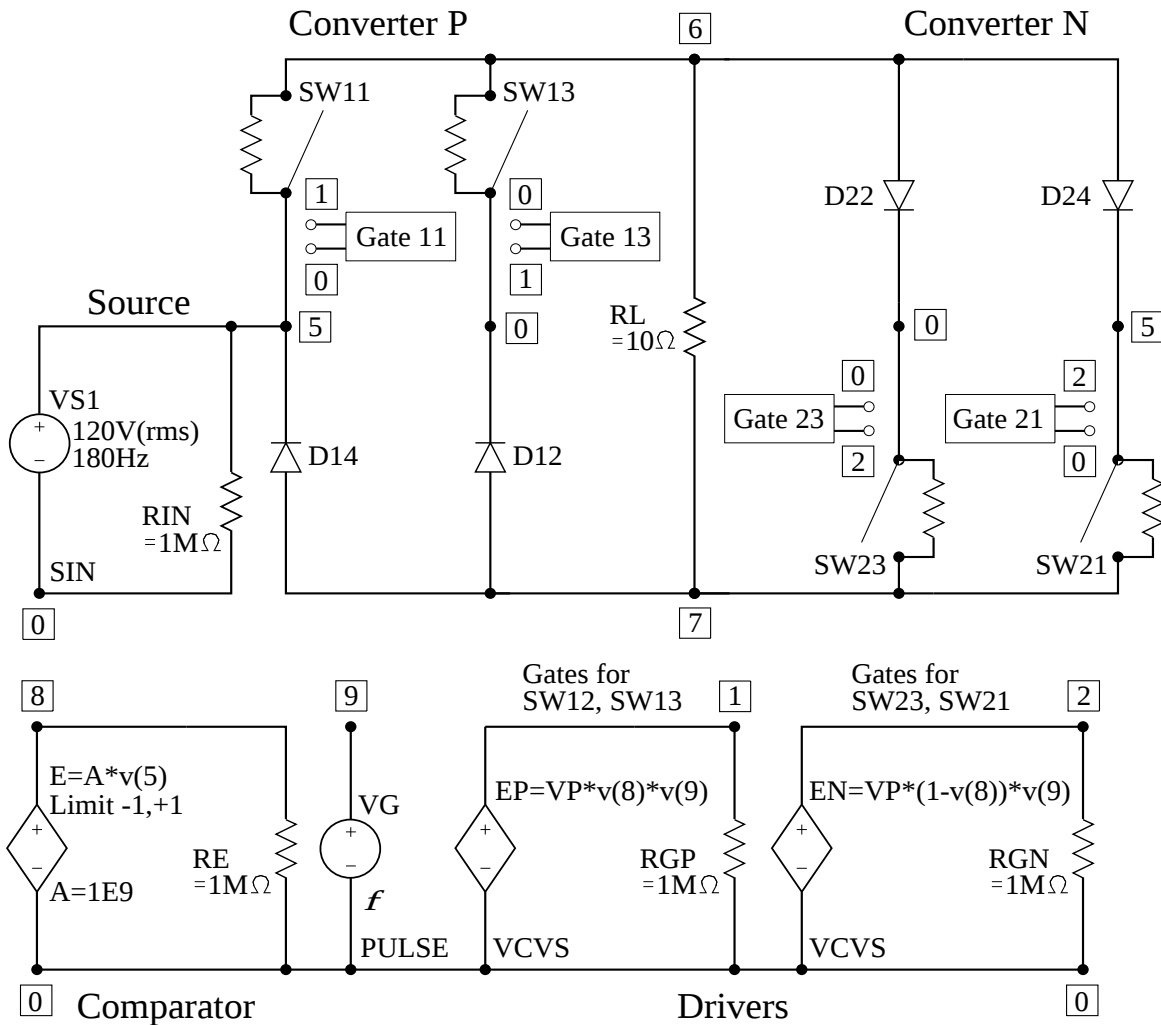


Fig. W9.3.3a PSpice configuration of a cyclconverter.

[illegible]

SINGLE-PHASE CYCLOCONVERTER WITHOUT MODULATION

* To determine the performance without voltage modulation.

.INC OPTIONS

* PARAMETERS

.PARAM	VS=120V	VMAX={SQRT(2)*VS};	Source voltage.
.PARAM	FREQ=150Hz	PERIOD={1/FREQ};	Supply frequency.
.PARAM	NUM=3	FREQC={FREQ/NUM};	Cycloconverter frequency.
.PARAM	PERC={1/FREQC};		Cycloconverter period.
.PARAM	VP=15V;		Gate signal nominal magnitude.
.PARAM	RLOAD=10ohms;		Load resistance.

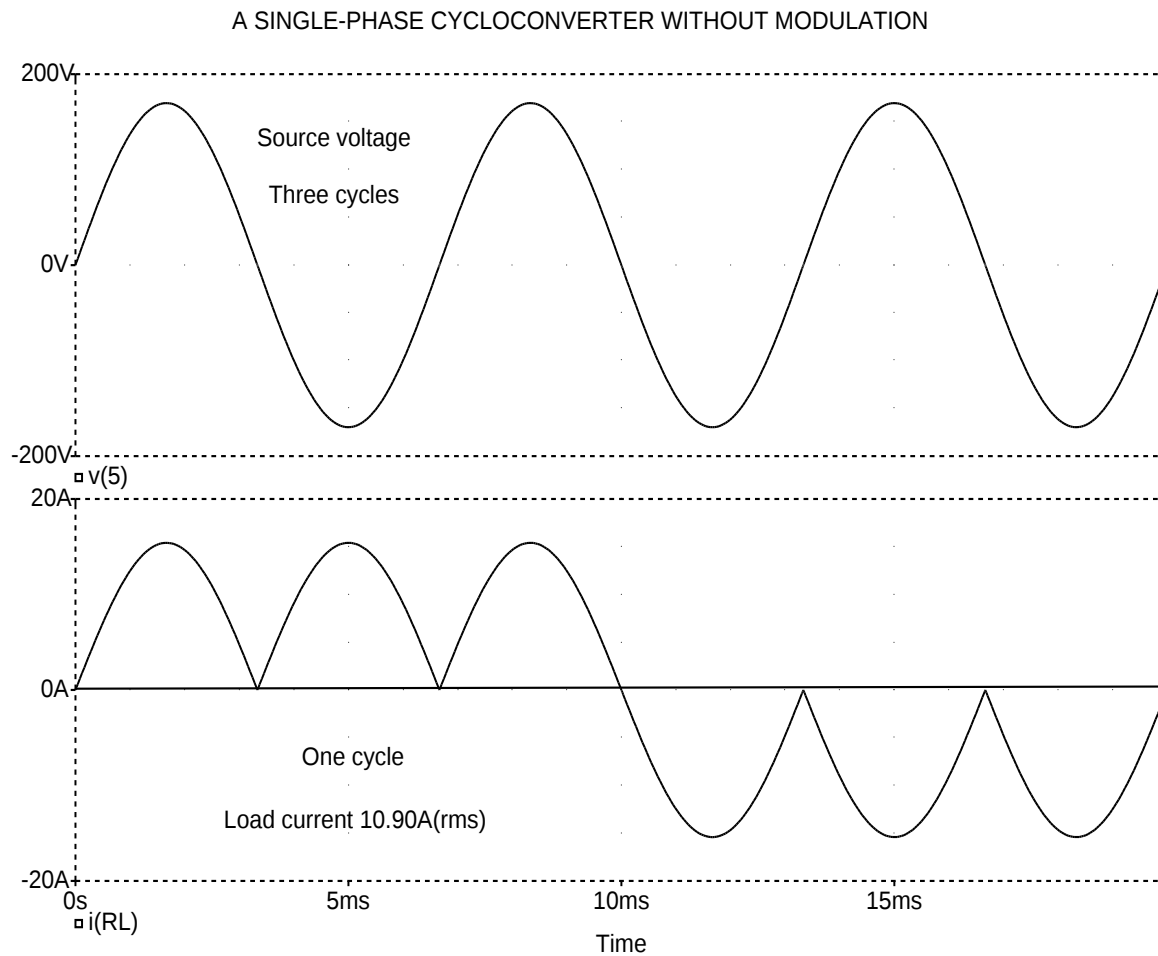


Fig. W9.3.3b

Part (a) of Solution. The average power P absorbed by the load is, from PROBE,

$$P = I_{l_{rms}}^2 R_l = 10.90^2 \times 10 = 1187 \text{ W}.$$

Part (b) of Solution. From the output file W9_3_3.OUT the total harmonic distortion THD of the load current waveform is $\text{THD} = 67.82\%$.

Part (c) of Solution. From W9_3_3.OUT, $I_{l1_{rms}} = 9.01 \text{ A}$.

Part (d) of Solution. From $\text{HF}_n = I_{ln} / I_{l1}$, the output file W9_3_3.OUT provides the data to give $\text{HF}_3 = 0.403$, $\text{HF}_5 = 0.5$, $\text{HF}_7 = 0.2$, $\text{HF}_9 = 0$.

END OF EXAMPLE W9.3.3

Drill Exercise WD9.3.3

The circuit diagram of a single-phase cycloconverter is shown in Fig. 9.3.3. The circuit has the following specifications.

$$V_s = 120\text{V(rms)} \text{ at } 60\text{Hz}, L_l = 0, R_l = 10\Omega, \\ \text{output frequency } f_o = 20\text{Hz}, \text{ delay angle } \alpha = 60^\circ.$$

(α is measured with respect to each half-wave input voltage.)

Follow the pattern of EXAMPLE W9.3.3 and do a PSpice simulation. Note that all output pulses constituting the output waveform are zero over the first third of their duration. Plot traces of the supply voltage and load current. Determine **(a)** the average power absorbed by the load, **(b)** the total harmonic distortion THD of the load-current waveform, **(c)** the fundamental rms value of the load current and **(d)** the harmonic factors HF of the third, fifth, seventh and ninth harmonics of the load-current waveform.

(Ans: **(a)** 955.3W, **(b)** 98.09%, **(c)** 6.84A, **(d)** 0.446, 0.70, 0.467, 0.127.)