Part 2 of Extra Material for use with

PSpice®
Simulation of Power Electronics Circuits

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Contents

See Appendix E in the book.

PSPICE SAWTOOTH GENERATOR

The sawtooth waveform is not a standard waveform in PSpice primitives. An approximate way to generate a sawtooth waveform is to use an independent-voltage PULSE source. The rise time would be just less than the period, for numerical reasons there must be a short pulse width, and the fall time TF would be very short. The sawtooth waveform is useful in driver circuits, so we will create a PSpice sawtooth generator in a subcircuit named VSAWTOOTH and write it in DRIVER.LIB. See Section 5.2.1, Fig. 5.2.3 (page 148 in the text).

EXAMPLE W5.2.1

Design a sawtooth generator with an output voltage of variable frequency and adjustable amplitude. Implement this generator simulation with an amplitude of 1V and a frequency of 100kHz. Write the circuit file with the sawtooth generator described in a subcircuit.

Solution

There are four steps in this solution.

STEP 1

A PSpice independent-voltage source can produce an approximate sawtooth waveform if the source is represented by a periodic pulse voltage. Figure W5.2.1 depicts a PSpice configuration and the waveform.

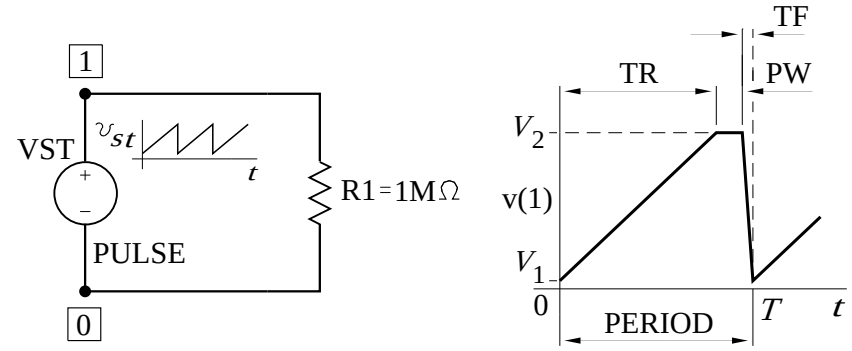

Fig. W5.2.1 Sawtooth generator.
(a) PSpice configuration, (b) waveform.

STEP 2 The circuit file is as follows.

» » » » » W5_2_1.CIR »

```
A SAWTOOTH GENERATOR NAMED VSAWTOOTH
* To plot a trace of the output-voltage waveform.
* Describe the generator as a subcircuit.
.SUBCKT VSAWTOOTH 101 100 PARAMS: VM=2V PERIOD=20us
* The subcircuit name is VSAWTOOTH. This is in DRIVER.LIB.
* The external nodes of the sawtooth voltage are 101, 100.
* Parameters (amplitude and period) are given default values.
VST 101 100 PULSE(0.01 {VM-0.01} 0 {PERIOD-2ns}
+                     1ns 1ns {PERIOD})
* V1=0.01V and V2={VM-0.01} ensures the full range of the duty cycle.
R1 101 100 1E6ohms
* Not really needed. PSpice puts 1/GMIN across sources.
.ENDS VSAWTOOTH;                    End of subcircuit description.
Xgenerator 1 0 VSAWTOOTH PARAMS: VM=1V PERIOD={PER}
* Nodes 1, 0 of the main circuit file correspond to 101, 100 in the subcircuit.
* The X statement calls for the subcircuit VSAWTOOTH.
* Its parameter values override the default values in the subcircuit.
* Needs a global parameter PER in the circuit file.
.PARAM   FREQ=100kHz  PER={1/FREQ}
.STEP    PARAM  FREQ  LIST  50kHz  100kHz
.TRAN    60ns  60us
.PROBE   v(1);                      Sawtooth-generator voltage.
.END
```

» »

STEP 3 A simulation of W5_2_1.CIR gives results similar to the ideal waveform shown in Fig. W5.2.1b with a period of 10µs and an amplitude of 1V.

STEP 4 See Fig. W5.2.1c. The subcircuit VSAWTOOTH is written in the library file DRIVER.LIB.

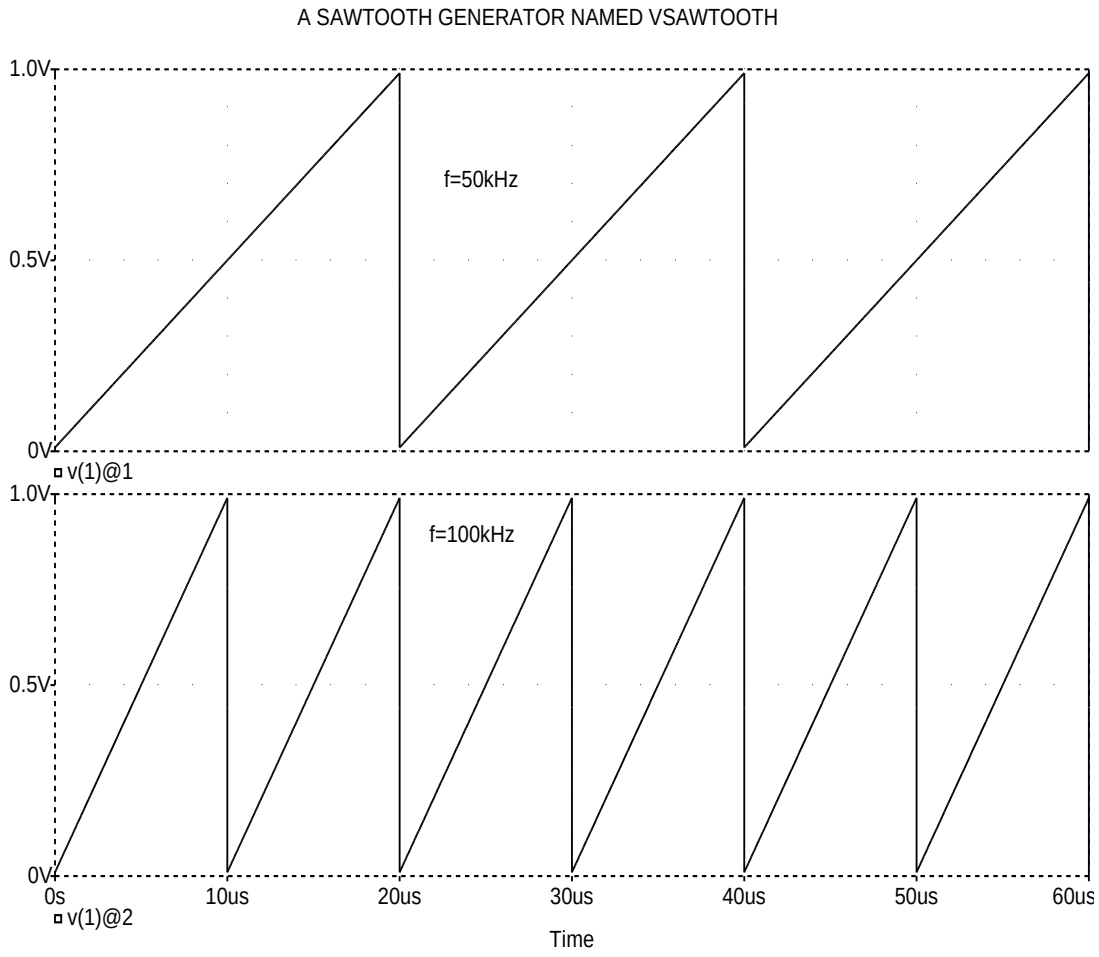

Fig. W5.2.1c

END OF EXAMPLE W5.2.1

COMPARATOR

For the duty-cycle control of a chopper, the comparator provides a gating signal that is adjusted by a reference voltage. See Section 5.2.1, Fig. 5.2.3 (page 148 in the text). The comparator is a straightforward device to use in a PSpice simulation, either by means of an analogue behavioural model (E source) or a macro model (subcircuit LM111). Reference can be made to Section 1.4 in Chapter 1 of the text. We have created subcircuits named COMPARATOR and COMPARATOR2 in DRIVER.LIB.

EXAMPLE W5.2.2

Design a comparator using an analogue behavioural model (E source) like that in Section 1.4. Include a 1% hysteresis and let the output voltage swing from ground level to the value of the positive op-amp source *VCC* = 15V. The input is a sinusoidal voltage of amplitude 2V and a frequency of 0.5Hz, as shown in Fig. W5.2.2a. Write the circuit file with the comparator described in a subcircuit. Plot traces of the input and output voltages. Check the hysteresis.

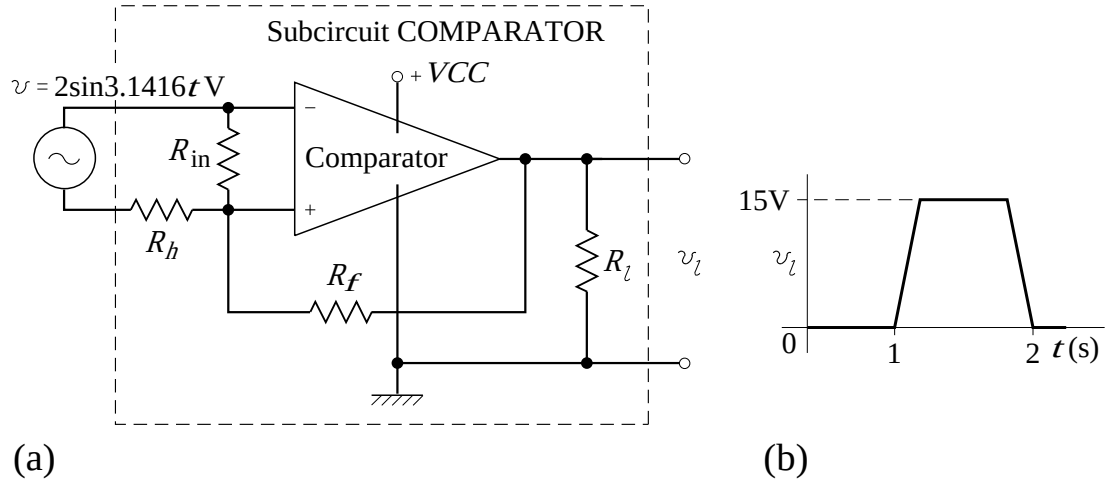

Fig. W5.2.2 A comparator with hysteresis.
(a) Circuit diagram, (b) output waveform.

Solution

In Section 1.4 of the text it was shown that a PSpice dependent source E together with a VALUE={LIMIT ... } expression can act as an analogue behavioural model of the comparator. If the noninverting input of the op-amp is greater than the inverting input, the output of the op-amp is finite but clipped at *VCC*. Otherwise, the output voltage is zero. There are four steps in this solution.

STEP 1 A PSpice configuration of the circuit is shown in Fig. W5.2.2c.

STEP 2 The circuit-file description of the PSpice configuration follows. The file includes the subcircuit COMPARATOR that is also written in the file DRIVER.LIB.

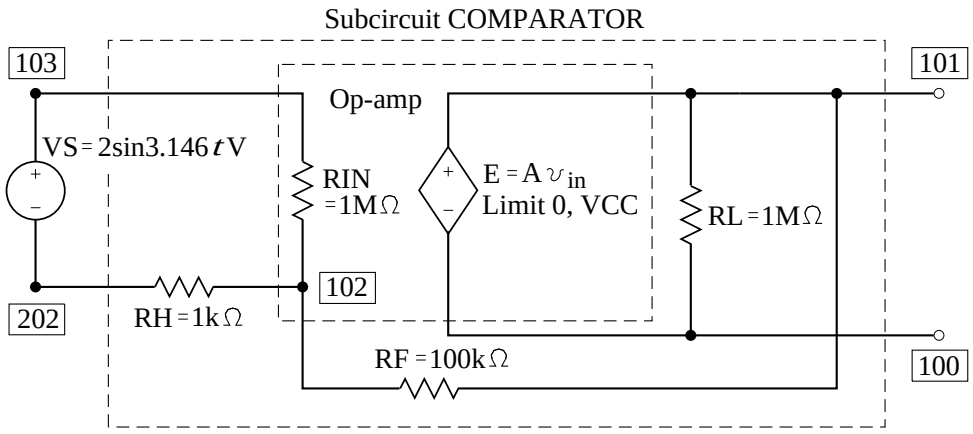

Fig. W5.2.2c PSpice configuration of a comparator.

» » » » » W5_2_2.CIR »

```
COMPARATOR MODEL FOR DRIVER.LIB
* To plot traces of input and output voltage waveforms.
* The comparator circuit is described as a subcircuit.
* This comparator has hysteresis.
* The only parameter is VCC, the positive source voltage.
* In terms of the op-amp in the subcircuit, the noninverting input is
* node 102 and the inverting input is node 103.
* The output node is 101, referenced to node 100.
* The gain in the linear region is A=1E5.
* Comparator is made "single-ended", negative-supply terminal is grounded.
* Op-amp output voltage vI=E1 clips at +VCC. E1 swings from 0 to VCC.

* This subcircuit is written to DRIVER.LIB
.SUBCKT COMPARATOR  202  103  101  100  PARAMS:  VCC=10V
E1   101   100   VALUE={LIMIT(V(202,103)*1E5, 0, +VCC)}
RF   101   102   100k;                 Positive feedback resistance.
RH   102   202   1k;                   "Hysteresis"resistance.
RIN  102   103   1E6;                  Op-amp input resistance.
RL   101   100   1E6;                  Op-amp output load resistance.
.ENDS      COMPARATOR

* Call for subcircuit into main circuit file.
* Needs a global parameter in the circuit file to define VGATE.
.PARAM       VGATE=15V
Xcomp   2   3   1   0   COMPARATOR  PARAMS:  VCC={VGATE}
VS   3    2    SIN(0  2V  0.5Hz);        Source across comparator input.
* Node 2 (noninverting), node 3 (inverting input).  1 output, 0 ground.
.TRAN        1ms     4.01s
.PROBE       v(1),   v(3, 2)
.END
```

» »

STEP 3 The PSpice simulation is run with the circuit file W5_2_2.CIR.

STEP 4 With PROBE, traces can be plotted of the input and output voltages of the comparator. This is shown in Fig. W5.2.2d. The results are virtually ideal. While the noninverting-input voltage of the comparator is greater than the inverting-input voltage, the comparator output is 15V. Otherwise the comparator output is zero.

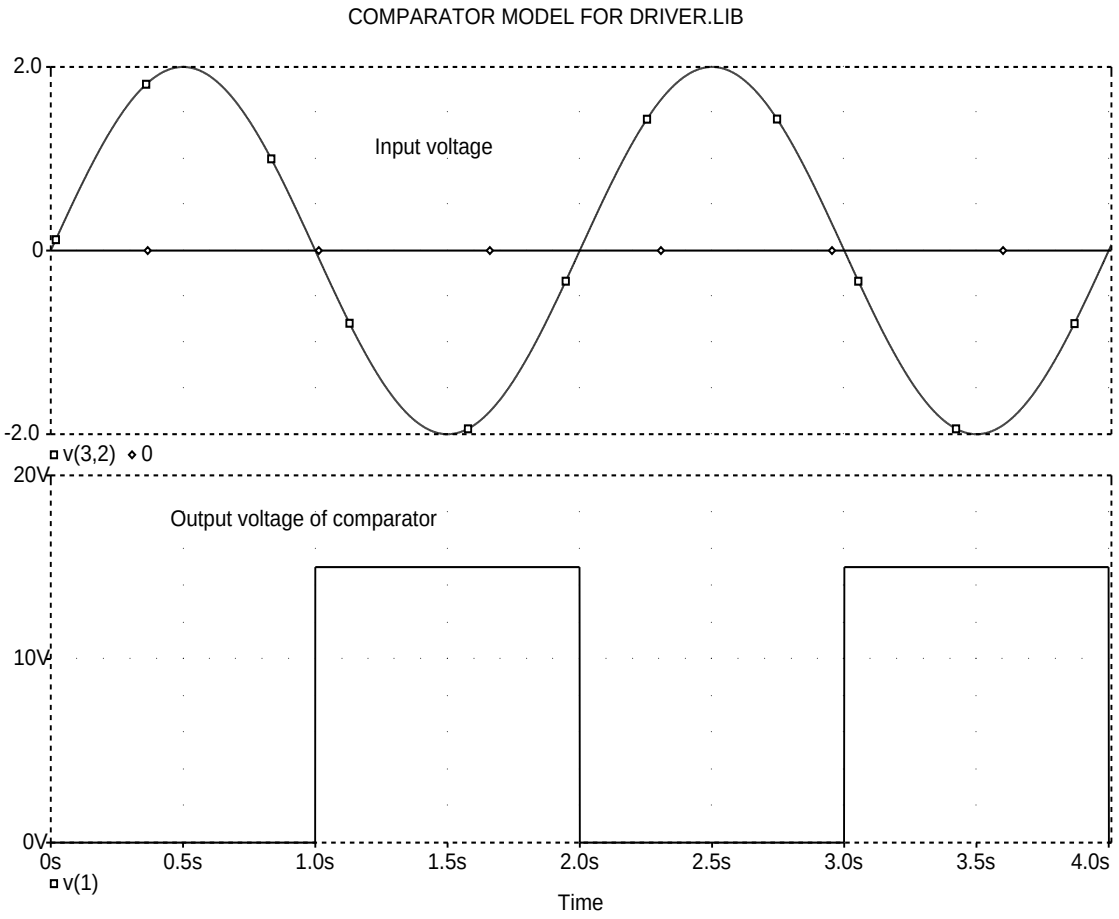

Fig. W5.2.2d.

END OF EXAMPLE W5.2.2

5.3.2 FULL-WAVE AC-DC CONVERSION

DELAY-ANGLE ALFA CONTROL

A topology for a single-phase, full-wave rectifier is in the form of a bridge with four power switches. This topology is illustrated in Fig. 5.3.3a. It is common for the switches to be thyristors which turn off naturally as the current falls to zero each cycle of the ac supply voltage.

During the half cycle of the ac-source voltage that rail A is positive, thyristors *TH*1 and *TH*2 are turned on at an angle α. While rail B is positive, thyristors *TH*3 and *TH*4 are turned on at an angle α. If the dc load is purely resistive all switches conduct for an angle $(\pi - \alpha)$ radians. If the equivalent load is inductive the conduction interval of the thyristors is greater than $(\pi - \alpha)$ radians. Also, if the equivalent load is capacitive the conduction interval is less than $(\pi - \alpha)$ radians.

For simulation, a gate signal to the switch for a duration $(\pi - \alpha)$ radians satisfies the requirements for a bridge with a resistive load. It is also satisfactory for an inductive load if the simulated switches are sensitive to current and switch off at current zero. A gate signal of $(\pi - \alpha)$ radians duration is not satisfactory for an equivalent capacitive load. Instead, a gate pulse of short duration, starting at α, must be used and the switch must be current sensitive; that is, the switch conducts only as long as there is current in it, even if the gate signal has been removed.

In this section we will only describe gate pulses of $(\pi - \alpha)$ duration. The switching of the thyristors in the above sequence, if the load is resistive, leads to a load-voltage waveform as shown in Fig. 5.3.3b.

The driver for a single-phase, full-wave bridge converter is more complex than the drivers considered so far. This is because there are four switches. All the switches must be controlled by the driver. However, the PSpice listing in the following example will be seen to be an extension of the listing for the half-wave converter. It will be found that there are two independent sources to control rectification of the positive and negative half cycles of the ac source. There are two dependent voltage sources that are added, so that the gate-drive signals for the switch pairs (*TH*1,*TH*2 and *TH*3,*TH*4) are isolated. Isolated drivers are often required for controlling actual semiconductor switches that are not *referenced* to ground.

In the following example, although thyristors *TH*1 and *TH*2 act in unison, their respective gate signals are at different potential levels above ground. Isolated (floating) drivers are easy to simulate in PSpice because of the availability of dependent-voltage sources.

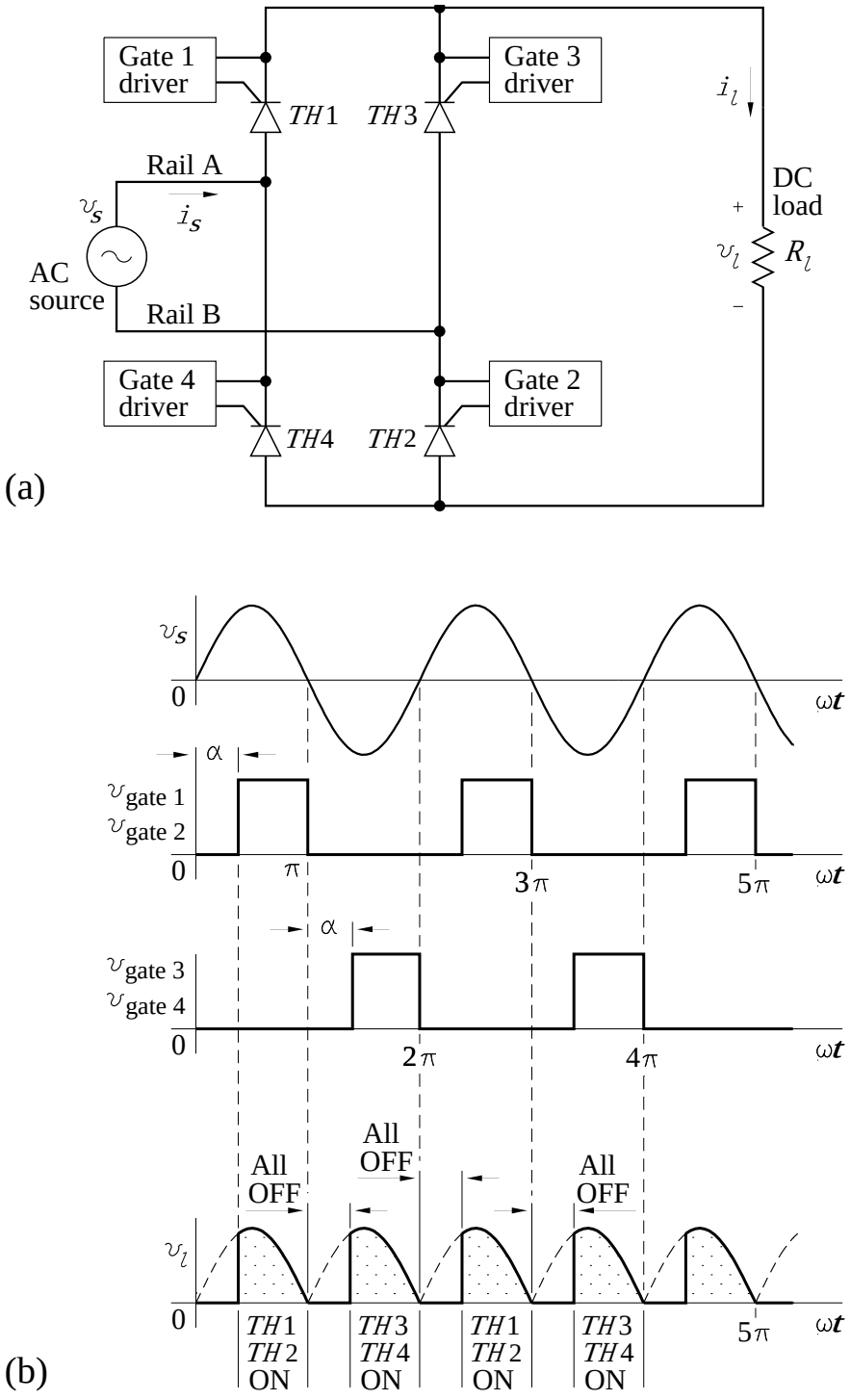

Fig. 5.3.3 A bridge rectifier.
(a) Circuit schematic, (b) waveforms for a resistive load.

EXAMPLE W5.3.1

Consider the circuit diagram in Fig. W5.3.1a. Simulate a driver for this bridge in a way that is suitable to write to DRIVER.LIB as a subcircuit. Use a sinusoidal voltage source of 240V(rms) at 50Hz as a reference and connect an arbitrary resistance of 1MΩ across it. The driver is to provide gate voltages of 5V to all four thyristors for intervals of $(\pi - \alpha)$ radians in the respective half cycles of source voltage. Let $\alpha = \pi/2$ radians and let each thyristor gate be modelled by a resistor of 50Ω. Plot traces of the reference sinusoid and all gate voltages over an interval of 60ms.

Solution

The solution is described in four steps.

STEP 1

From Fig. W5.3.1 and the specifications, a PSpice configuration of the drivers and the reference voltage can be drawn. This is shown in Fig. W5.3.1a. It is created to have the four gate signals described within a subcircuit. All nodes in PSpice must have a dc path to ground. Consequently, the high-side cathode terminals of the two gates are connected to ground through 10MΩ resistors.

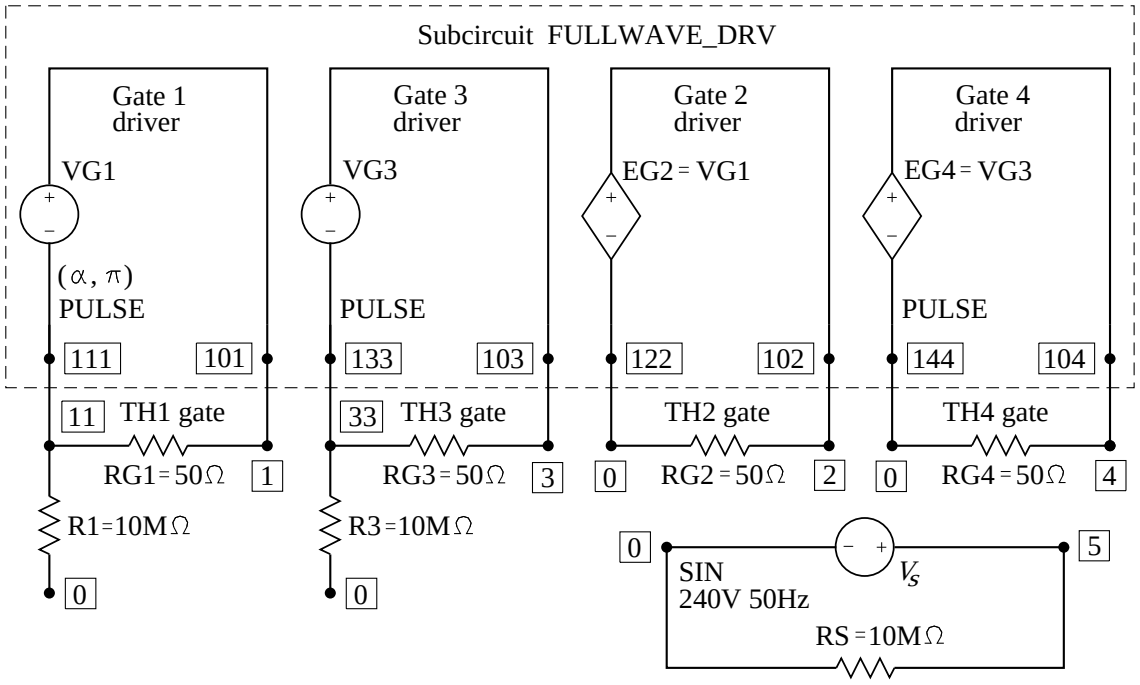

Fig. W5.3.1a Full-wave PSpice configuration.

STEP 2

From the PSpice configuration, shown in Fig. W5.3.1a, a circuit file named W5_3_1.CIR can be written so that the driver is in the form of a subcircuit.

If the general circuit comprising the source, converter, load and driver contains too many nodes (24) for the evaluation version to handle, we can dispense with the dependent sources in the simulation.

STEP 3

The PSpice simulation is run with circuit file W5_3_1.CIR. The gate voltages generated by the driver and the sinewave reference voltage are recorded. The job time was about 17.3s.

» » » » » W5_3_1.CIR »

```
DRIVER FOR A SINGLE-PHASE FULL-WAVE CONTROLLED RECTIFIER
* To plot the driver output waveforms for ALFA=90° and FREQ=50Hz.

* PARAMETERS needed in the main circuit for the subcircuit.
.PARAM    VGATE=5V    VSIN=240V        VMAX={1.414*VSIN}
.PARAM    FREQ=50Hz   PERIOD={1/FREQ}
.PARAM    ALFA=90;                     In degrees.

* SOURCE.    Sinewave reference.
VS  5    0    SIN(0  {VMAX}  {FREQ})
RS  5    0    1E7ohms;                 To close the voltage source loop.

* A SUBCIRCUIT DRIVER NAMED FULLWAVE_DRV.
* Nodes 101, 111 and 102, 122 have voltages to control
* switches TH1 and TH2.
* Nodes 103, 133 and 104, 144 have voltages to control
* switches TH3 and TH4.
.SUBCKT  FULLWAVE_DRV  101  111  102  122  103  133  104  144
VG1      101   111  PULSE(0  {VGATE}  {PERIOD*ALFA/360}
+        1ns   1ns  {PERIOD*(180-ALFA)/360}  {PERIOD})
VG3      103   133  PULSE(0  {VGATE}  {PERIOD*(180+ALFA)/360}
+        1ns   1ns  {PERIOD*(180-ALFA)/360}  {PERIOD})
EG2      102   122  (101, 111)   1;          A voltage identical to VG1.
EG4      104   144  (103, 133)   1;          A voltage identical to VG3.
.ENDS FULLWAVE_DRV

* CIRCUIT ELEMENTS
RG1      1     11    50;          Model of thyristor TH1's gate resistance.
RG2      2     0     50
RG3      3     33    50
RG4      4     0     50
R1       11    0     1E7ohms;           To give a dc path to ground.
```

```
R3        33     0      1E7ohms
Xdriver  1       11     2    0     3      33   4      0   FULLWAVE_DRV
* A call for the subcircuit named FULLWAVE_DRV.
* Main-circuit nodes 1, 11, 2, 0, 3, 33, 4, 0, correspond to
* subcircuit nodes 101, 111, 102, 100, 103, 133, 104, 100.

. TRAN      0.2ms     60ms
. PROBE    v(1, 11),  v(2),   v(3, 33),   v(4),    v(5) ;       Four gate voltages.
. END
```

» »

STEP 4

From PROBE, the traces of the gate voltage to each thyristor for $\alpha = \pi/2$ radians are plotted together with the reference sinewave. This is shown in Fig. W5.3.1b.

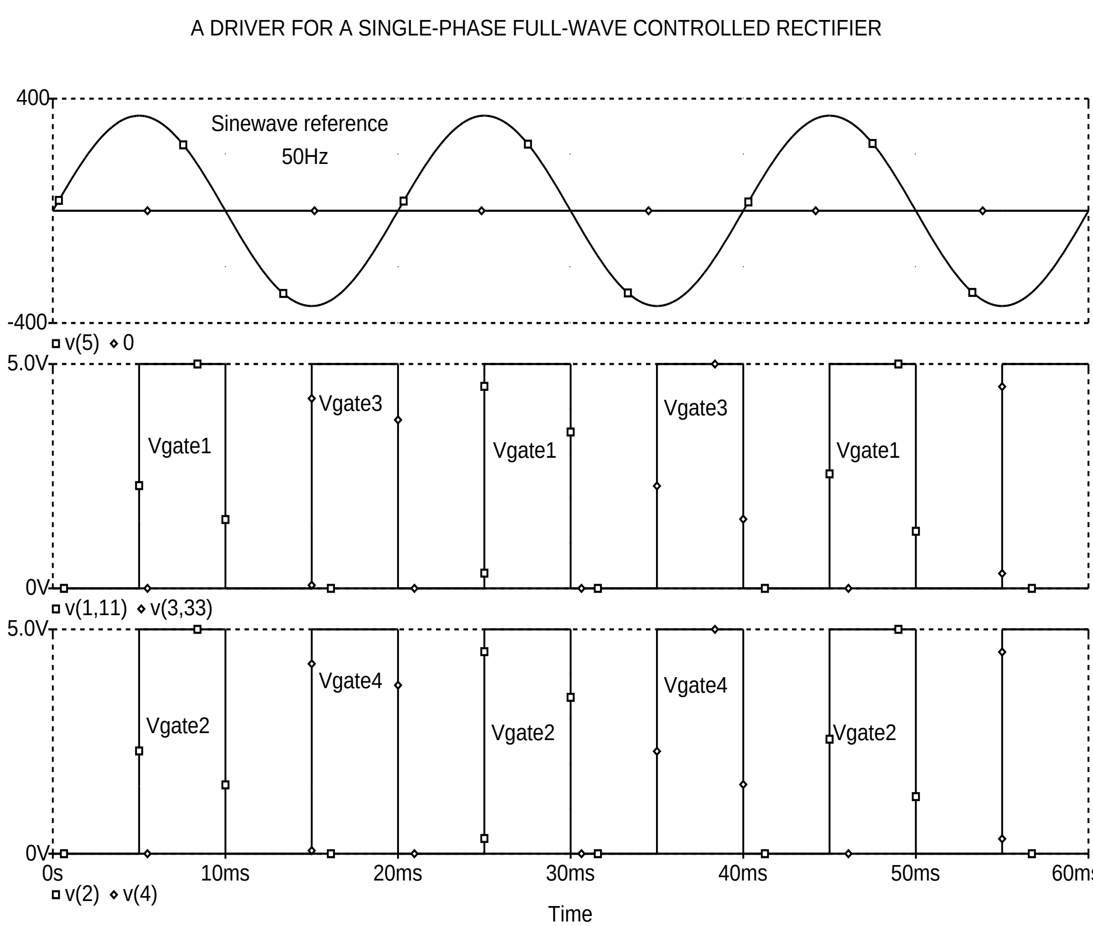

Fig. W5.3.1b

END OF EXAMPLE W5.3.1

Drill Exercise WD5.3.1

Following the pattern of EXAMPLE W5.3.1, simulate a driver of a single-phase, full-wave, thyristor-controlled, bridge rectifier. The ac source has a voltage of 240V(rms) at 60Hz. The gate voltages of the thyristors are limited to 6V and the delay angle is $\pi/6$ radian. Resistances of 100Ω can model the driver loads. Plot traces of the sinewave reference voltage and the voltages across thyristors *TH*2 and *TH*4 over an interval of 50ms.

Drill Exercise WD5.3.2

Use the subcircuit named FULLWAVE_DRV in the file DRIVER**.**LIB to simulate a driver for a single-phase, full-wave, controlled bridge rectifier. The driver is to generate the four gate voltages with respect to a 100-V(rms), 100-Hz sinewave reference. The 4-V gate voltages are to be turned on with a delay angle of ALFA = 40 degrees. Assume a reasonable value for any elements that are used to complete the circuit. Plot the gate voltages and the sinewave reference over an interval of 40ms.

5.4.4 DIGITAL DRIVER (SPWM)

Many driver switching schemes have been devised in the quest to obtain an inverter ac waveform that closely resembles a sinewave. One technique is to extend the method of equal multiple pulses described in Section 5.4.3 in the text. The extension is to modulate the width of the pulses over the half cycle of the gate signal. This can be called a modulating PWM driver. We will consider the single-phase bridge inverter whose schematic diagram is shown in Fig. 5.4.1 in the text. The switches are driven in pairs *Sw*1, *Sw*2 and Sw3, *Sw*4. Our aim in this section is not to design switching strategies for a PWM driver, it is to exemplify a technique that can be simulated using PSpice.

EXAMPLE W5.4.1

Design an SPWM modulator using the 555 timer IC. The driver circuit is to provide modulating 12-V gate signals for an output frequency of 60Hz. The carrier frequency is to be 2kHz. Do a PSpice simulation and plot traces of the carrier signals, the reference signal for modulation and the PWM gate signal over one modulating cycle.

Solution

In EXAMPLE 5.2.3 the 555 timer was used in the astable mode as a driver for a chopper. In this example we will use the 555 timer in the monostable mode (one shot) as a driver for an inverter. Further, the pulse widths of the gate signals will be modulated over each period of the output cycle. This is done to improve the performance of the inverter output.

Figure W5.4.1a shows the external connections of the 555 timer for the monostable mode of operation. The 555 timer generates one output pulse every time a short pulse (going negative) is applied to the trigger input (pin 2). The width of the input pulse must be less than the width of the output pulse. The width of the output pulse is set by the *RC* timing network. When the trigger input goes low, the output (pin5) goes high and the timing capacitor *C* begins charging at an exponential rate set by the *RC* time constant. When the capacitor voltage exceeds the control voltage on pin 5, the 555 timer resets. This reset action causes the discharge of the timing capacitor. Thus, the output (pin5) goes low until another trigger pulse occurs. The 0.01μF capacitor, that is connected to pin 5, decouples and filters internal circuitry. Once a trigger pulse is applied, the output pin goes high and the timer capacitor charges at the rate

$$v_6(t) = V_{CC}\left(1 - e^{-t/RC}\right). \qquad (5.4.4)$$

The output pin remains high until the lapsed time t_p at which the capacitor voltage v_6 equals the control voltage v_5. Thus,

$$v_6(t_p) = v_5 = V_{CC}\left(1 - e^{-t_p/RC}\right). \tag{5.4.5}$$

$$\text{Therefore, } t_p = RC \ln\left(\frac{V_{CC}}{V_{CC} - v_5}\right). \tag{5.4.6}$$

There is the special case where no external reference control voltage is applied to pin 5. In this case $v_5 = 2V_{CC}/3$ internally, so $t_p \approx 1.1RC$.

This was used in EXAMPLE W5.3.2 in Section 5.3.3 on the WEBsite.

Pulse width-modulation is the practice of generating a continuous stream of pulses whose width can be modulated. For chopper drivers, PWM (pulse-width-modulation) meant that the stream of gate pulses had a constant width ($m = t_{ON}/T =$ constant), but the pulse width could be changed (adjustable duty cycle m). For inverters we want a modulating PWM signal. That is, the many gate pulses per cycle have the pulse width varied from a small value, to a large value and back to a small value over the cycle.

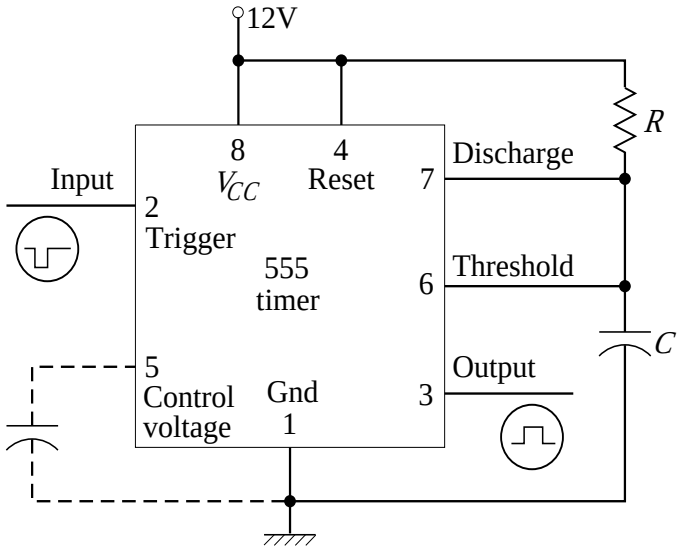

Fig. W5.4.1a
Monostable mode.

This modulating PWM action can be achieved by the 555 timer. An external sinusoidal voltage at pin 5 can create the modulation by changing the point at which the capacitor voltage resets the timer. This voltage at pin 5 is the SPWM reference voltage for modulation. Clock pulses at pin 2 can continuously retrigger the timer for one-shot pulses at the desired frequency (2kHz). These clock pulses constitute the carrier signal for modulation.
The solution of this example is done in five steps.

STEP 1

The first step in the solution is to determine the values of the external elements of the 555 timer according to the specifications of the required operation.

The gate signal is to have a magnitude of 12V. Therefore, we provide a timer voltage source $V_{CC} = 12\text{V}$.

Let us choose the source of modulation, connected to the control-voltage pin (5), to be a sinewave that arbitrarily has a range of 2V to 10V (always positive, but less than V_{CC}). The 10V level represents 100% modulation (max. pulse width). For accurate modulation we will select an *RC* time constant such that the capacitor voltage v_6 just reaches 10V during the period T_p of the pulse source at the input trigger pin (2). (This source is a *clock* with a frequency $f = 2\text{kHz}$).

Using eq. (5.4.6) with $t_p = T_p = 1/f = 500\mu\text{s}$

$$RC = 500 \times 10^{-6} / \ln(6) = 0.279 \times 10^{-3} = 0.279 \text{ ms.}$$

Let $C = 0.1\mu\text{F}$. Consequently, $R \approx 2.8\text{k}\Omega$.

There are two points to note.

1. There is not an exact linear relationship between the control voltage v_5 and the pulse width ($t_{ON} = mT_p$) of the output voltage v_3, because the voltage rise across the capacitor is exponential.
2. It is not possible to obtain a zero pulse width ($m = 0$) for the output pulse v_3, since the minimum output pulse width is limited by the trigger pulse width. Thus, the trigger pulse width must be kept short. In this example, we have chosen a trigger pulse width of 10μs which is short compared with the period $T_p = 500\mu\text{s}$.

In summary

$$R = 2.8\,\text{k}\Omega, \quad C = 0.1\mu\text{F}, \quad V_{CC} = 12\text{V}, \quad v_5 = (6 + 4\sin 377t)\text{ V},$$

$$v_2 = 12\text{V} \quad (t_{ON} = 10\mu\text{s},\ f = 2\text{ kHz},\ m = 0.02).$$

STEP 2

From the circuit diagram in Fig. W5.4.1a and from the design data above a PSpice configuration of the PWM driver can be drawn. This is shown in Fig. W5.4.1b.

STEP 3

The PSpice configuration in Fig. W5.4.1b can be used to compose a circuit file. The circuit file is named W5_4_1**.**CIR and its description is as follows.

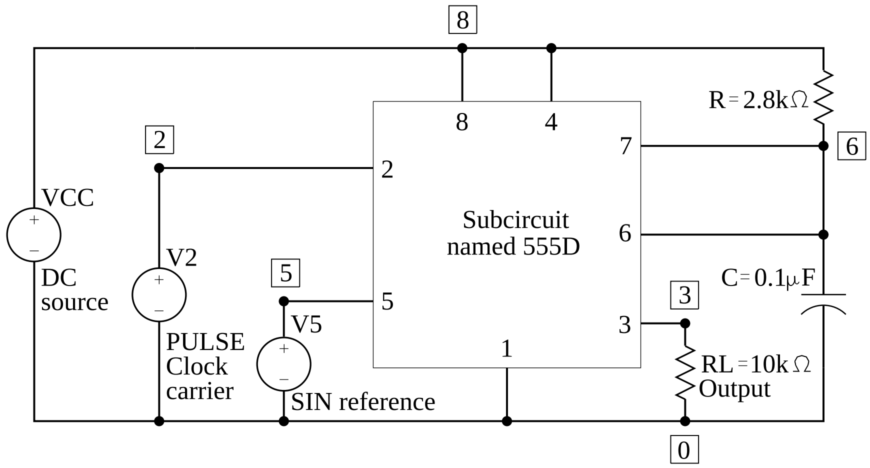

Fig. W5.4.1b PSpice PWM driver configuration.

» » » » » W5_4_1.CIR »

SPWM INVERTER DRIVER (555 TIMER)
* To plot a trace of the modulating gate pulses.

* PARAMETERS

```
.PARAM  VC=12V;                        Timer voltage source.
.PARAM  TON=10us;                      Carrier pulse width.
.PARAM  PWMFREQ=2kHz  PER={1/PWMFREQ}; Carrier frequency.
.PARAM  FREQ=60Hz;                     Inverter modulating frequency.
.PARAM  VHI=10V  VLO=2V;               Range of reference modulating voltage.
.PARAM  VDC={VHI/2+VLO/2};             DC offset of reference voltage.
.PARAM  VMAX={VHI/2-VLO/2};            Amplitude of reference signal.
```

* SOURCES

```
VCC  8  0  DC  {VC};                   This source voltage is for the 555 timer.
V2   2  0  PULSE({VC} 0 0 1ns 1ns {TON} {PER});  Carrier voltage.
V5   5  0  SIN({VDC} {VMAX} {FREQ});   Reference sinewave.
```

* Use the evaluation library for the 555 timer subcircuit.

```
.LIB  EVAL.LIB
```

* Call the subcircuit 555D in the monostable configuration.

```
XTIMER  0 2 3 8 5 6 6 8  555D;         Subcircuit named 555D.
R       8 6  2.8kohms;                 Timing resistor.
C       6 0  0.1uF;                    Timing capacitor.
RL      3 0  10kohms;   Equivalent resistance of the driver output gate.
```

```
* ANALYSIS, over one cycle of modulation.
. TRAN     100us   17ms
. PROBE    v(3),     v(2),    v(5) ;        Output, carrier and sinewave voltages.
. END
```

» »

STEP 4

The PSpice simulation can be run with the circuit file W5_4_1.CIR. The results are stored in a data file named W5_4_1.DAT.

STEP 5

Using PROBE we can plot traces of v(2), the carrier wave (clock), v(5), the modulating wave (reference), and v(3), the PWM output gate voltage. Figure W5.4.1c shows these waveforms. They illustrate the effectiveness of the simple 555-timer pulse-width modulator that may serve well for a number of applications.

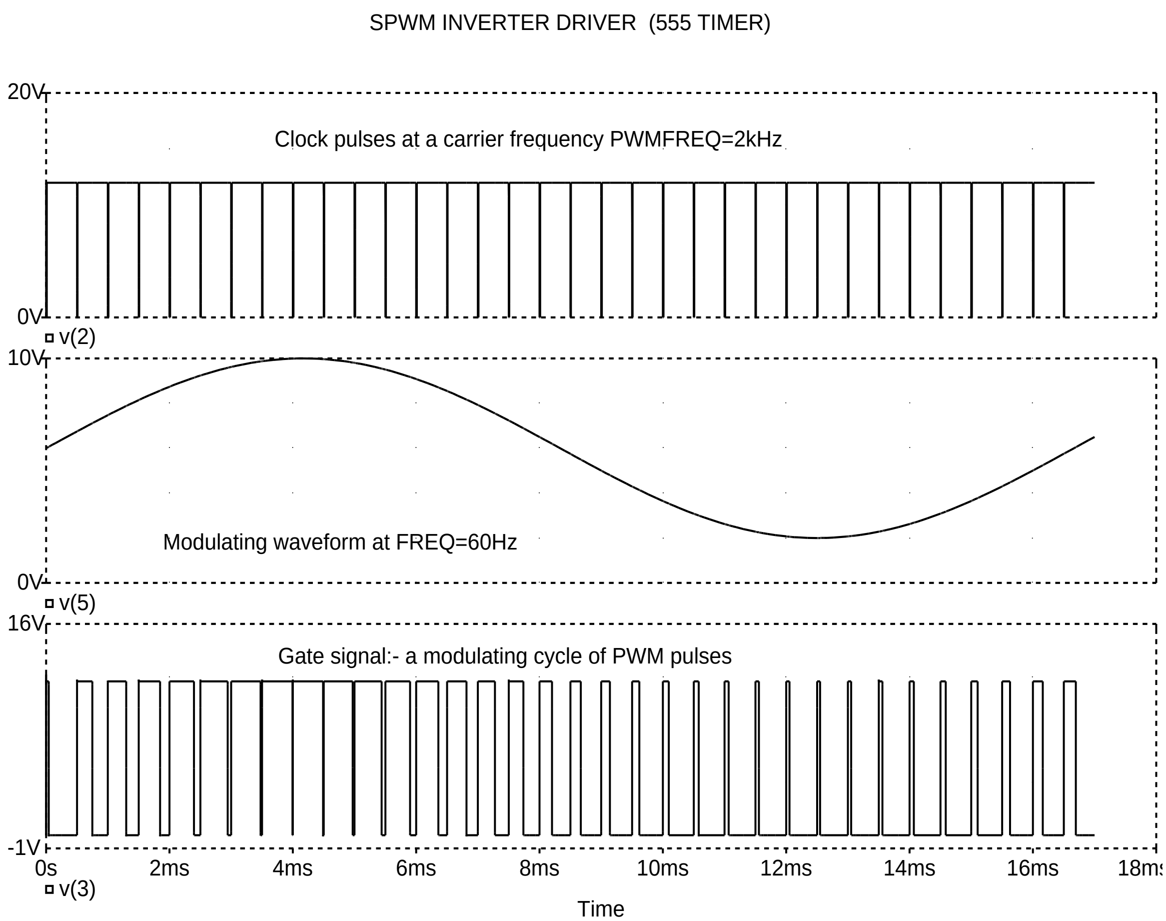

Fig. W5.4.1c

END OF EXAMPLE W5.4.1

Drill Exercise WD5.4.1

Design a modulating PWM driver using a 555 timer IC. The specifications are that the gate pulses have a magnitude of 12V, the modulating signal is to be a sinewave of frequency 50Hz and there are to be 20 gate pulses per modulating cycle. Do a PSpice simulation and plot traces of the carrier signals, the modulating signal and the output gate signals.