Part 1 of Extra Material for use with

PSpice®
Simulation of Power Electronics Circuits

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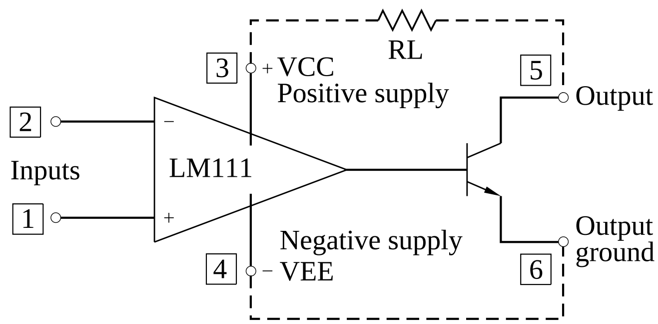
Contents

See Appendix E in the book.

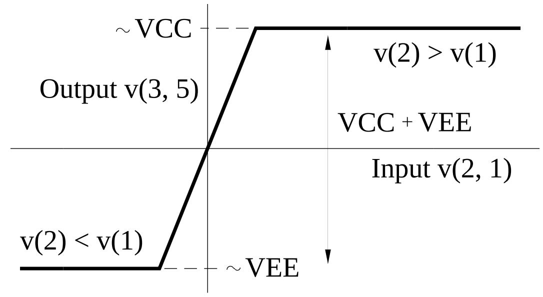
1.4.4 PSPICE COMPARATOR MACRO MODEL

The use of an analogue behavioural model (VCVS E) has proved to give near-ideal results of a comparator in Section 1.4.3. Job times were short and few nodes were needed. The comparator has a macromodel built into PSpice's library file EVAL.LIB. Inspect it; it models the comparator LM111, a silicon monolithic integrated circuit suitable for driving lamps, relays and solenoids. It is found in EVAL.LIB in a subcircuit with the name LM111. See Fig. 1.4.4.



(a)

Fig. 1.4.4 The LM111 comparator.
(a) PSpice configuration,
(b) characteristics.



(b)

```
* Refer PSpice to the appropriate library file.
. LIB        EVAL.LIB

* The next statement calls the comparator model into the circuit file.
Xcomparator    1   2   3   4   5   6   LM111 ;      X signifies a subcircuit.
*     |        |   |   |   |   |   |     |
*     |        |   |   |   |   |   |     Subcircuit name in library.
*     |        |   |   |   |   |   Output ground.
*     |        |   |   |   |   Node for output.
*     |        |   |   |   Node for negative supply, VEE.
*     |        |   |   Node for positive supply, VCC.
*     |        |   Node for inverting input connection (−).
*     |        Node for noninverting input connection (+).
* Device name in main circuit.
* The node numbers can be arbitrary.  The order of the comparator
* connections is important.
```

These statements will be recognised in the example that follows.

There are several different ways to use the LM111 comparator. A common way is to treat the comparator as an open-collector output. The output-ground pin is connected to the system ground or VEE. The load is connected between the output pin and VCC. BJT turn-on occurs if the noninverting input voltage v(1) is less than the inverting input voltage v(2). Turn-on in accompanied by (VCC + VEE) appearing across the load resistor RL. Otherwise, the voltage across the load is virtually zero.

The load resistance value has to be set so that the load current does not exceed 50mA. Too high a value for R_l results in a slow voltage rise-time as the output "floats" high.

EXAMPLE W1.4.4

Repeat EXAMPLE 1.4.3 of the text using the PSpice comparator, model LM111. Use the load connection shown in Fig. 1.4.4 with a load value $R_l = 500\Omega$. Plot the traces of the input and output-voltage waveforms. Note the job time.

Solution

There are four steps to achieve a solution.

STEP 1

From Fig. EX1.4.3a we can draw the PSpice configuration using the subcircuit LM111 to represent the comparator. See Fig. 1.4.4.

STEP 2

From the PSpice configuration in Fig. 1.4.4 and the description of the comparator as a subcircuit above, we can write a circuit file W1_4_4.CIR. See next page.

STEP 3

The PSpice simulation is run with the circuit file W1_4_4.CIR. The results, input and output voltages as functions of time, are written in the file W1_4_4.DAT for the use of PROBE.

STEP 4

We can use PROBE to create traces of the sinusoidol input voltage v(2, 1) and the output voltage v(3, 5) as shown in Fig. W1.4.4 on the next page. As expected, if v(2) > v(1) the output voltage v(3, 5) is 30V. Otherwise, the output voltage is zero. With this macro model LM111 the output-voltage rise-time is 8ms, but the fall-time is 30ms. These are slow responses. The job time was 9.62s, almost two seconds less that the job with the analogue behavioural model in EXAMPLE 1.4.3.

» » » » » W1_4_4.CIR »

```
LM111 COMPARATOR FOR ZERO-CROSSING DETECTION
* To determine the input and output waveforms.

* SOURCES
VS        2    1    SIN(0  1V  1Hz);              Input voltage.
VCC       3    0    DC     15V;                   Device positive source.
VEE       0    4    DC     15V;                   Device negative source.

* CIRCUIT ELEMENT and DEVICE
RL        5    3    500 ohms;     Load resistance between collector and VCC.
Xcomparator         1  2  3  4  5  4  LM111;      Subcircuit call.

* Subcircuit for library file.
. LIB     EVAL.LIB

* ANALYSIS
. TRAN      3ms      1.6s
. PROBE     v(2, 1),    v(3, 5);     To view input and output voltages.
. END
```

» »

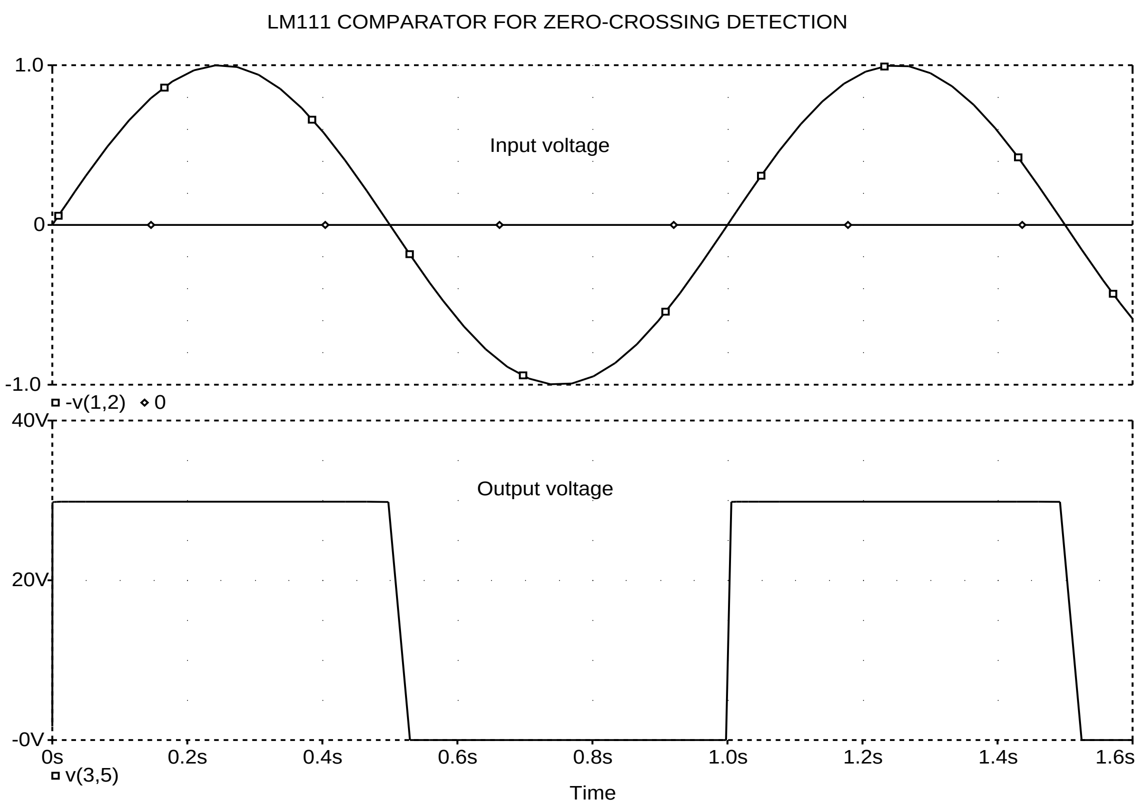


Fig. W1.4.4

END OF EXAMPLE W1.4.4

Drill Exercise WD1.4.1

Repeat Drill Exercise D1.4.5 (in the text) using the comparator LM11 from the file EVAL.LIB, but changing the load resistance to $R_l = 500\Omega$. Compare the results.

Drill Exercise WD1.4.2

Repeat Drill Exercise D1.4.6 using the comparator LM111 from the file EVAL.LIB and having a load resistance $R_l = 500\Omega$. Compare the results.

Drill Exercise WD1.4.3

Repeat Drill Exercise D1.4.7 using the comparator LM111 from the file EVAL.LIB, and having a load resistance $R_l = \Omega$. Compare the results.

2.4 AC-AC MODULATION SIMULATION

One form of ac-ac power modulation is voltage regulation, keeping the output-voltage frequency of the power-electronics circuit equal to the input-voltage frequency. In power-electronics terms this type of modulation is referred to by a variety of different names such as point-on-wave switching, or trigger-angle control, or firing-angle control, or delay-angle control, or ac-line phase control. They all mean the same thing. At low power levels ac-voltage regulation is accomplished in practice using a triac switch. We will use a generic form of a switch for simulation. See Fig. 2.4.1a.

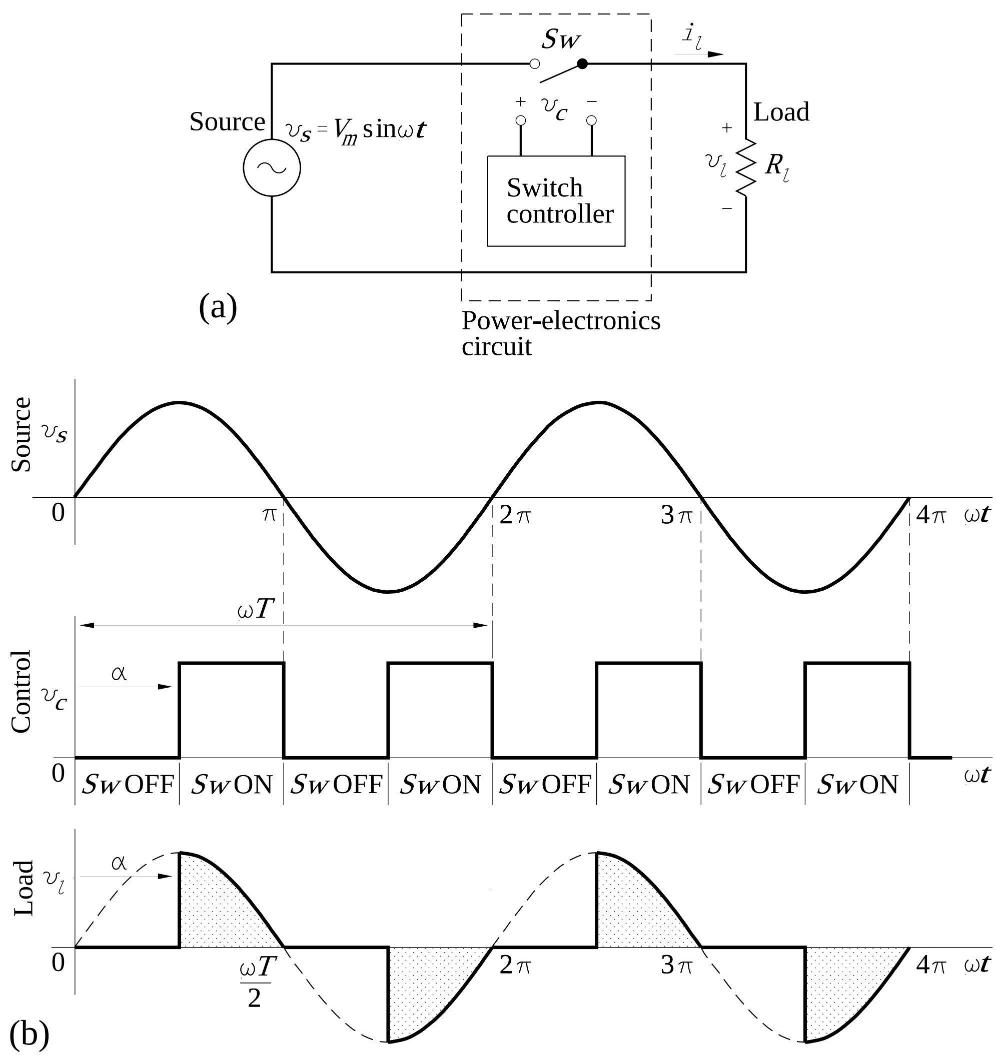


Fig. 2.4.1 An ac-voltage regulator.

Figure 2.4.1a illustrates a circuit comprising an alternating-voltage source v_s, a load resistor R_l and a power-electronics circuit to modulate the load power. The power-electronics circuit is a voltage-controlled switch *Sw* that turns on and off at the same point on the supply waveform each cycle. The turn-on points can be adjusted.

The voltage-controlled switch is controlled by the voltage source v_c that is generated by a supply to have periodic pulses. The period is half that of the power source. If the control voltage is $v_c = \text{VON}$ the switch is in the on-state. If the control voltage is $v_c = \text{VOFF}$ the switch is in the off-state. Figure 2.4.1b shows the voltage waveforms for a general delay angle $\alpha + n\pi$ for turning the switch on and an extinction angle $n\pi$ for turning the switch off. The integer n is 1, 2, 3, ... What can be seen from Fig. 2.4.1b is that the rms value of the load voltage v_l is adjusted by altering the firing angle α. For the range of the firing angle $0 \le \alpha \le \pi$ the load voltage varies from $V_m/1.414$ to zero.

2.4.1 AC-VOLTAGE REGULATION

The power-electronics circuit for ac-voltage regulation is similar to the dc-chopper circuit. In this case the switching frequency of the chopper is fixed at twice the frequency of the voltage source.

EXAMPLE W2.4.1

Consider the circuit diagram of Fig. 2.4.1. The purpose of the circuit is to modulate the power in a load by adjusting the rms value of the ac voltage that is applied to the load. The switch *Sw* controls the point-on-wave that the input voltage $v_s = 240\sin 314t\,\text{V}$ appears across the output terminals. The load resistance is $R_l = 10$ ohms. Use PSpice and PROBE to give plots of the output current i_l for switch trigger angles α of 0 and 1.0 radian with the extinction angle set at π and repeated every half cycle of the input voltage waveform.

Solution

We will generalize the circuit file so that the program can be used for different voltage sources, switch firing angles and load resistances. This is accomplished by using parameters and expressions.

STEP 1

The first step is to configure a circuit diagram for PSpice. This is shown in Fig. W2.4.1a.

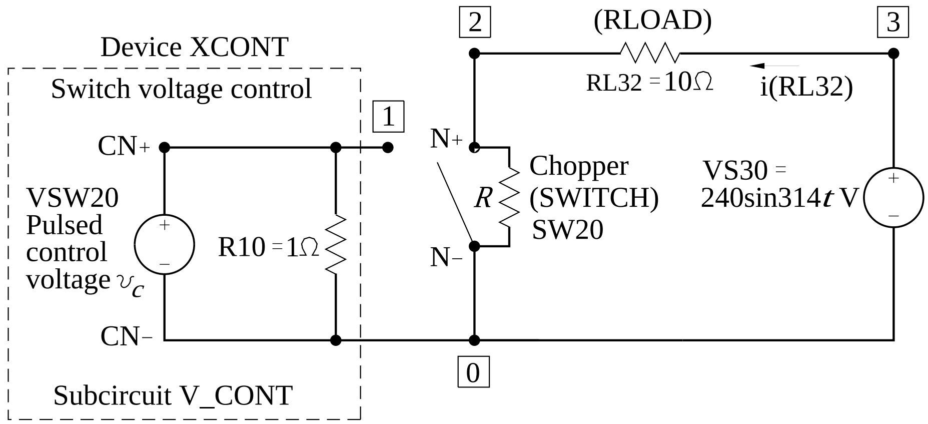


Fig. W2.4.1a PSpice configuration of a voltage regulator.

STEP 2 The second step involves writing the circuit file from the PSpice circuit configuration that was done in Step 1. The circuit file, listed on the next page, includes a subcircuit for the control-voltage (or driver) circuit. The subcircuit is defined in Fig. 2.4.1a, Fig. W2.4.1a and in the library file POWER.LIB under the name V_CONT (for voltage_control).

Note the use of expressions in this circuit file. This simplifies editing for the same circuit configuration with different parameter values.

Expressions {...} cannot be used in the .STEP statement or in the .TRAN statement.

In this circuit file there is a control statement with the dot command .OPTIONS. NOPAGE is an option to suppress paging and certain section headers in the output file to save space.

RELTOL = 0.01 is an option that stipulates a calculation of variables to 1% accuracy (default 0.1%). This saves time of the program execution.

The device XCONT is the subcircuit named V_CONT that defines the voltage-control circuit for turning on and off a switch of the model type VSWITCH. The subcircuit is described in the library file POWER.LIB and is repeated here.

```
. SUBCKT   V_CONT     101     100
VSW20      101        100
+ PULSE(0  1  {DELAY}  1ns  1ns  {PERIOD/2 - DELAY}  {PERIOD/2})
R     101  100        1ohm
. ENDS     V_CONT
```

```
»»»»» W2_4_1.CIR »»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»
AC-VOLTAGE REGULATOR
* Determine current responses for different values of firing angle ALFA.
* This regulator uses a voltage-controlled switch as an ac chopper.
* Include the power-electronics library and define parameters.
.LIB POWER.LIB;                              A library call.
.OPTIONS NOPAGE RELTOL=0.01;                 A control statement.

* PARAMETERS
.PARAM FRE=50Hz;       This is the voltage source frequency parameter.
.PARAM RLOAD=10ohms;                   This is the load resistance.
.PARAM PI=3.14159,  TWOPI={2*PI};      Note the expression {...}.
.PARAM ALFA=0rad;                      The firing angle α.
.PARAM DELAY={ALFA/(TWOPI*FRE)};       Firing angle in seconds.
.PARAM VRMS=240V, VMAX={SQRT(2)*VRMS};RMS and amplitude.
.PARAM PERIOD={1/FRE};                 Period of the supply voltage.

* SOURCE, a sinusoidal voltage in the power circuit.
VS30 3  0  SIN(0 {VMAX} {FRE});        Note the expressions {...}.

* Call a subcircuit named V_CONT from the library file.
XCONT  1  0  V_CONT;          Subcircuit controlling the switch.

* DEVICE
SW20    2  0  1  0  SWITCH;            A voltage-controlled switch.

* If there is no model statement for SWITCH PSpice does a library call.
* CIRCUIT ELEMENT
RL32    3  2  {RLOAD};                 This is the load resistor.

* Perform a multiple run for different values of firing angle.
.STEP  PARAM  ALFA  LIST  0  1;               α=0 and α=1rad.

* ANALYSIS, transient, to view the load current.
.TRAN  20us  30ms;            TSTEP=20μs, TSTOP=1.5cycles.

* OUTPUT
.PROBE i(RL32);  Graphics postprocessor to view load current only.
.END
»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»
```

STEP 3

The third step is to run the PSpice simulation with the circuit file W2_4_1.CIR. The results of the transient analysis for the load current i(RL32) are stored in the data file. The results cover the two runs, one for α=0 and one for α=1.0rad.

STEP 4

The fourth step is to view the traces of the load current for the two runs using the PROBE postprocessor. We will plot the results on two graphs to show the differences in the current responses for the two cases of the firing angle, α=0 and α=1.0rad. The plots of a transient analysis automatically have the *x*-axis scaled for time. ALFA in the .STEP statement is in radians. However, the DELAY parameter makes a conversion of the firing angle to time and DELAY in used in the control-voltage subcircuit named V_CONT.

Let us go into the PROBE environment with the file W2_4_1.DAT.
From the display menu we click on **All_transient_analysis** (or hit **A**).
PROBE sets up the data structure and loads the data.
From the new display menu we click on **Add_trace** (or hit **A**).
Then, we follow the prompt, and key in i(RL32)@1. This gives us the trace of the first run (@1 is for α=0).
From the new display menu we click on **Plot_control** (or hit **P**).
From the new display menu we click on **Add_plot** (or hit **A**).
We get a second trace and a new menu.
Click on **Exit** (or hit **E** or **ESC**).
From the new display menu click on **Add_trace** (or hit **A**).
For a second time we follow the prompt, but this time we key in i(RL32)@2. This gives us the trace of the second run (@2 is for α=1rad).
One trace† is illustrated in Fig. W2_4_1b, depicted on the next page.
Using the firing angle α as a controlling variable we can adjust the alternating-voltage output of this regulator circuit. The output waveform is periodic but it is also distorted from the ideal sinusoid that occurs only for α=0. PSpice can help us determine not only the true rms value of the voltage waveform for any α, it can also provide information about how much distortion there is.

† It is an option in PROBE to load the results of all runs. Hitting **Add_trace** and typing i(RL32) causes the waveforms from all runs to be displayed. This option is meant to be used in Extra Drill Exercise ED3.2.2 on the WEBsite.

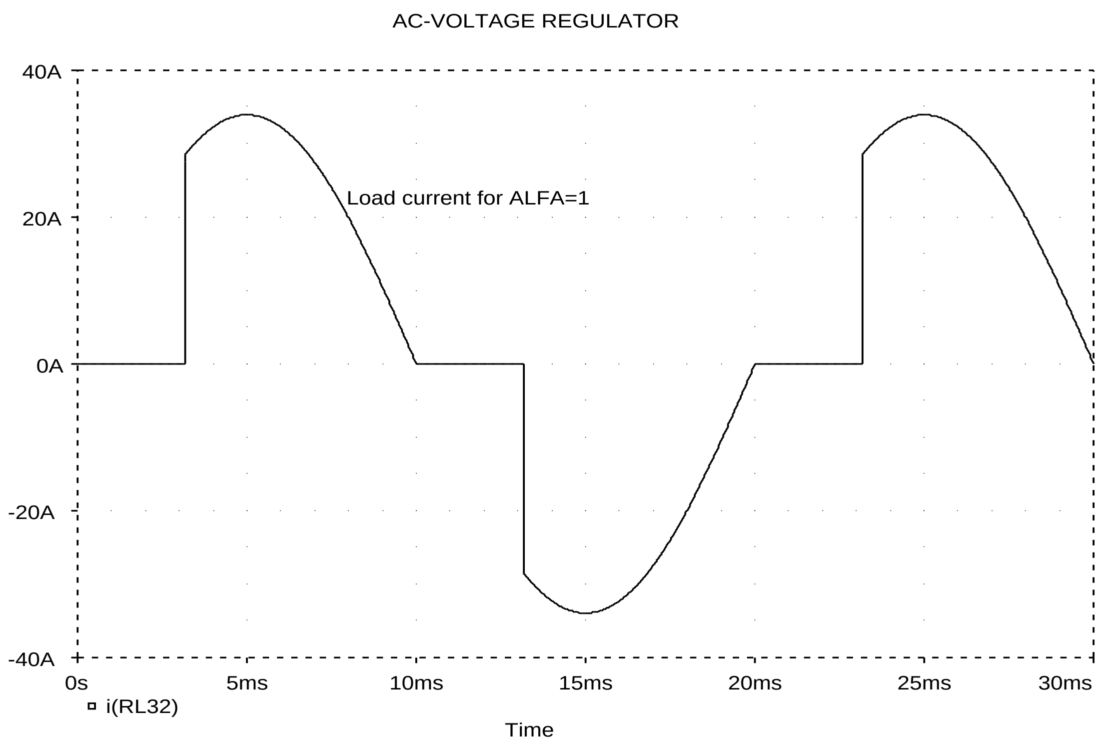


Fig. W2.4.1b

END OF EXAMPLE W2.4.1

Drill Exercise WD2.4.1

Use the information given in Fig. W2.4.1a for an ac-voltage regulator. From a PSpice simulation plot the waveform of the ouptut v(3, 2) for the firing angles $\alpha = \pi/6$ rad and $\alpha = \pi/2$ rad using the .STEP command for multiple runs.

Drill Exercise WD2.4.2

An ac-voltage regulator in the form of a voltage-controlled switch is illustrated in Fig. 2.4.1. The voltage source has the form $v_s = 169.7 \sin 377t$ volts and the load resistance has a value $R_l = 5.0$ ohms. Use a single PSpice simulation and PROBE to determine the load-current waveforms for firing angles $\alpha = 0$ and $\alpha = \pi/2$ radians. The control-voltage subcircuit named V_CONT in the library file POWER.LIB can be used.

Drill Exercise WD2.4.3

Consider the circuit diagram in Fig. 2.4.1. The voltage-controlled switch modulates power from the 240-V(rms), 100-Hz supply to a 30-Ω resistive load. The modulation is accomplished by point-on-wave control, both turn-on (alpha) and turn-off (beta). If $\alpha = \pi$ radian and $\beta = 2\pi/3$ radians, determine the load voltage trace by PSpice simulation.

4.2.2 CURRENT-CONTROLLED SWITCH AS THE DIODE

A PSpice current-controlled switch (symbol W, model type ISWITCH) can represent the ideal diode. See Table W4.2.1. Together with this switch we use a current sensor in the form of a voltage source which has a zero-voltage magnitude.

EXAMPLE W4.2.2

A circuit diagram, comprising an ac source, a half-wave rectifier and an *RL* load, is shown in Fig. W4.2.2a. Obtain a PSpice configuration of this circuit using a current-controlled switch to model the ideal diode. Use PROBE to view the diode current and voltage waveforms.

Solution

There are four steps in this solution.

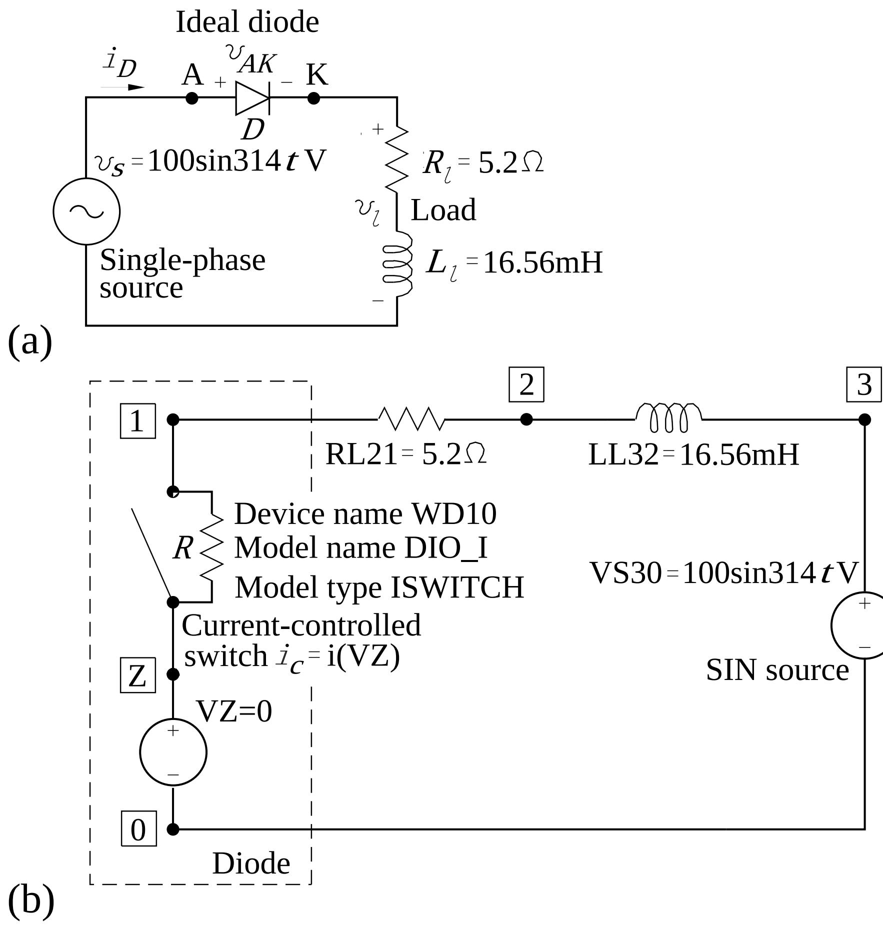


Fig. W4.2.2 Half-wave rectifier.
(a) Circuit diagram, (b) PSpice configuration.

STEP 1 The first step involves transforming the circuit diagram in Fig. W4.2.2a to a PSpice configuration as in Fig. W4.2.2b. The current-controlled switch is the model of the diode. The switch's statement name is WD10, the model name is DIO_I, the model type is ISWITCH and the control current is $i_c = i_D \equiv$ i(VZ).

STEP 2 The second step is to use the PSpice configuration to create a circuit file. The circuit file is shown on the following page. There is a small design exercise involved in order to determine appropriate values of the switch parameters. You may like to adjust these values to obtain results that are closer to those of an ideal diode.

```
»»»»» W4_2_2.CIR »»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»
DIODE TEST CIRCUIT FOR MODEL  DIO_I
* Compare characteristics of a current-controlled switch with an ideal diode.
* The switch is to turn on if the current (or voltage) in it is positive and the
* switch is to turn off if the current (or voltage) tends to reverse.

* SOURCE
VS30   3    0    SIN(0  100V  50Hz);      Sinusoidal voltage supply.

* CIRCUIT ELEMENTS
RL21   2    1    5.2ohms;                 Load resistance.
LL32   3    2    16.56mH;                 Load inductance.

* CIRCUIT DEVICE
* This is a current-controlled switch that models the diode.  It has a data
* statement and a model statement.
WD1Z   1    Z    VZ     DIO_I; . . . . . . . . . . . . . . . . . . . . . . . . . . (1)
.MODEL  DIO_I  ISWITCH(RON=1E-3  ROFF=1E6
+                       ION=0  IOFF=-1E-4); . . . . . . . . . . . (2)

* CURRENT SENSOR for PSpice.
VZ  Z  0  0V; An independent-voltage source across (Z, 0) of zero volts.

* ANALYSIS, always in the transient mode.
.TRAN  20us  30ms  0   40us
* Analysis covers 3 half cycles. TMAX=40µs.
.PROBE
.END
»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»»
```

EXPLANATION OF THE FILE W4_2_2.CIR

There are two new statements in this file. They are in lines (1) and (2).

. . . .

Line (1) of circuit file W4_2_2.CIR

```
WD1Z   1     Z    VZ     DIO_I;                                  (1)
```

- This is a statement of a device. In this case it is a statement of a current-controlled switch (W).
- There are four fields in this statement.
- The first field is for the name of the switch WD1Z. The name must begin with a W since the switch is current controlled. The rest of the name is arbitrary.
- The second field contains the names (1, Z) of the nodes to which the switch is connected.
- The third field contains VZ which is the name of a voltage source. It is this source that PSpice uses to sense the control current. It must be a voltage source. We have designated the voltage of the source VZ to be zero so that it does not affect the circuit in any way. An ideal voltage source has no impedance. Therefore, there is no voltage drop across VZ. For a diode model the source VZ is connected in series with the switch so that both source VZ and switch WD1Z have the same current.
- The fourth field contains DIO_I, which is the arbitrary model name of the diode, and which links the device data statement with the .MODEL parameter description.

. . . .

Line (2) of circuit file W4_2_2.CIR

```
.MODEL  DIO_I  ISWITCH(RON=1E-3  ROFF=1E6
+                         ION=0  IOFF=-1E-4);                    (2)
```

- This is the model statement that gives a description of the device parameters.
- There are four fields in this statement.
- The first field contains .MODEL. This provides PSpice with the information that device parameter values are to follow.
- The second field contains DIO_I which is the model name of the device, linking it with device data statements that have the same name in the fourth field.
- The third field contains ISWITCH which is the model type of the current-controlled switch.

- The fourth field contains (RON = 1E−3 ROFF = 1E6 ION = 0 IOFF = −1E−4). The parameters RON and ROFF are the on-state resistance and off-state resistance of the switch respectively. ION and IOFF are the control current values (in this case i(VZ)) that cause the value of the switch resistance *R* to be RON and ROFF respectively.
  For the range ION ≥ i(VZ) ≥ IOFF the value of the switch resistance lies in the range RON ≤ *R* ≤ ROFF. Figure W4.2.2c depicts the characteristics of the switch. If any of the parameter values in the model statement are omitted, PSpice assumes default values. Default values are given in Table W4.2.1.

Fig. W4.2.2c
Characteristics of a current-controlled switch.

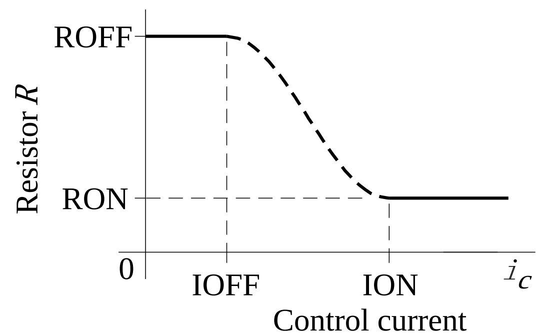


Table W4.2.1 Model parameters of the current-controlled switch (Model type ISWITCH)

Model parameter	Description	Units	Default value
RON	Resistance of the closed switch	ohms	1Ω
ROFF	Resistance of the open switch	ohms	1MΩ
ION	Minimum control current to close the switch	amperes	1mA
IOFF	Maximum control current to open the switch	amperes	0

- The choice of the parameter values is as follows. RON = 1E−3Ω, ROFF = 1E6Ω, ION = 0, IOFF = −1E−4A. Initially, the condition of the circuit is that the circuit current is zero and the voltage is rising positively, so the switch is on. If we had required the current to be ION = 1μA before the switch turned on, there would have been convergence problems in the numerical analysis.

The maximum circuit current is about 15A, so the maximum model-diode voltage drop while conducting is 15mV. This is close to being ideal.
After the source voltage reverses polarity the current will fall to zero and reverse. We do not want reverse current in the diode, so ideally IOFF would be zero. This cannot be so, because of the choice of ION. Since $|ION - IOFF|$ must be a reasonable value to prevent PSpice convergence problems, we set $IOFF = -0.1mA$. At this value of current the resistance of the diode rises to $ROFF = 1M\Omega$. There will always be a negative value of current to maintain the diode off until the supply causes the voltage to become positive again. At this point the cycle of events repeats.
In the choice of the resistance values, keep the ratio ROFF/RON less than 10^{12}.

This ends the explanation of circuit file W4_2_2.CIR

. . . .

STEP 3 The third step is to run the PSpice simulation for file W4_2_2.CIR.

STEP 4 The fourth step is to run PROBE and view the current and voltage of the diode model in this rectifier circuit. The results, as shown in Fig. W4.2.2d, on the next page, look like the expected results of a virtually ideal 100-V, 15-A rectifier circuit with inductance. The inductance makes the current lag the voltage of the supply so that there is a diode current for a part of the cycle that the supply has a reverse-polarity voltage. The results here are smoother than those obtained with a voltage-controlled switch. This suggests that the spikes of voltage, obtained in EXAMPLE 4.2.1 in the text, were due to the step changes of current with the numerical analysis. The step ceiling of 40μs (TMAX) that was used in the transient analysis of this example is too low to eliminate the voltage spike at the current discontinuity. The same comment applies to a printing step size $TSTEP = 10\mu s$ (20μs is much better). When the switch turned off, the current discontinuity required an analysis step size of about 10^{-12} s.

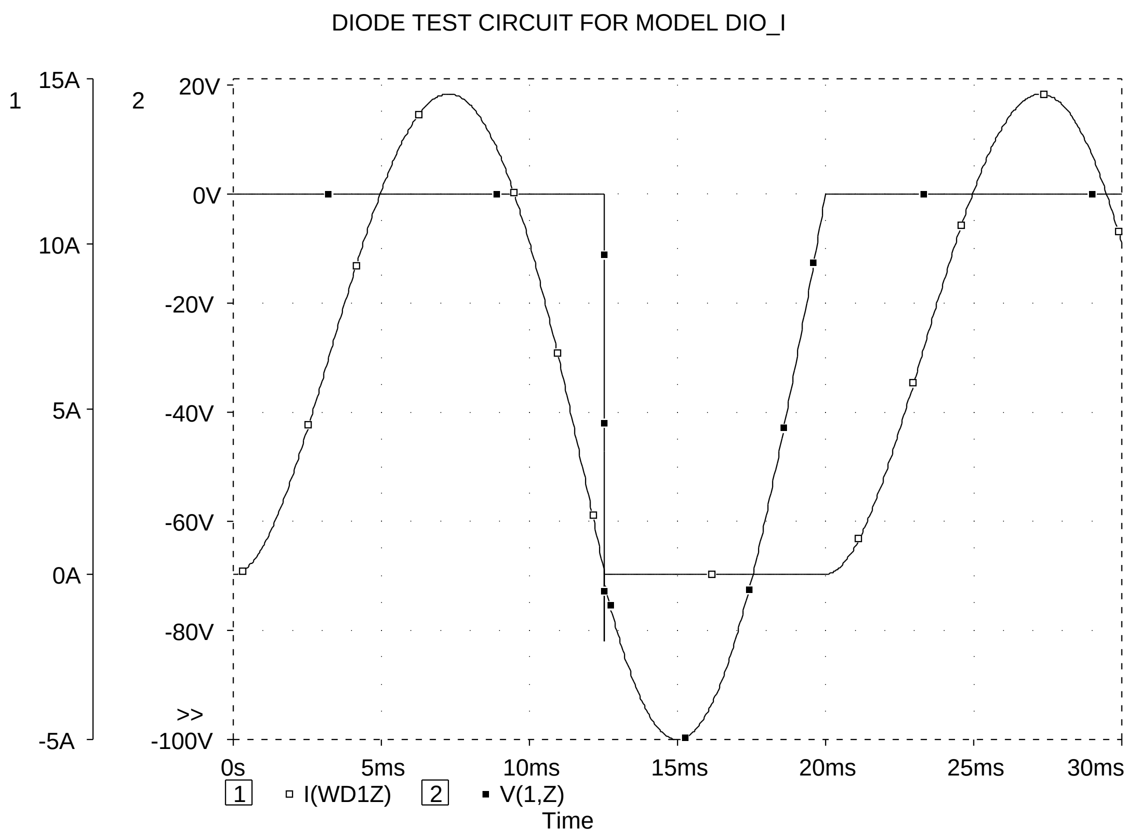


Fig. W4.2.2d

END OF EXAMPLE W4.2.2